

FIG. 1A

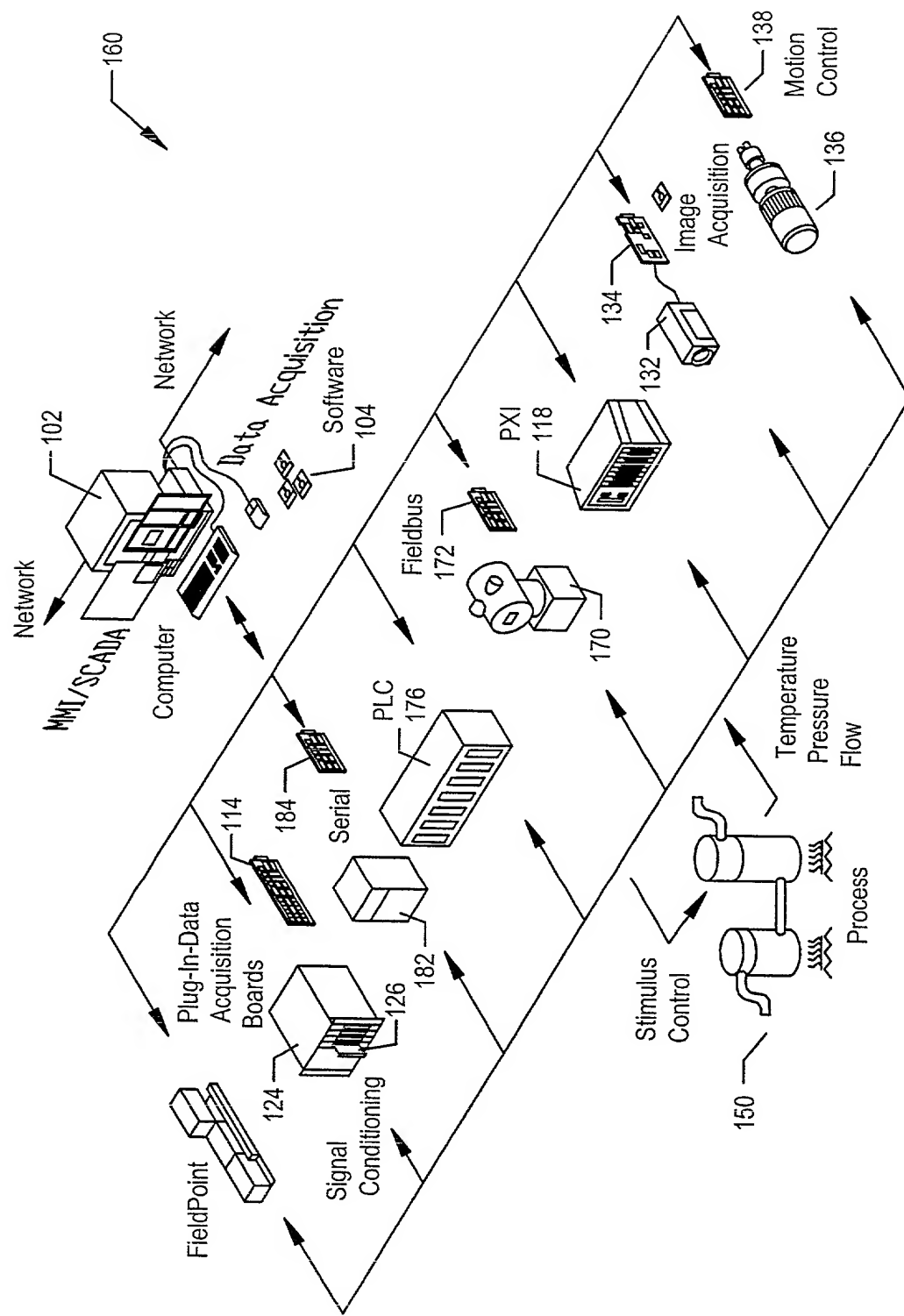


FIG. 1B

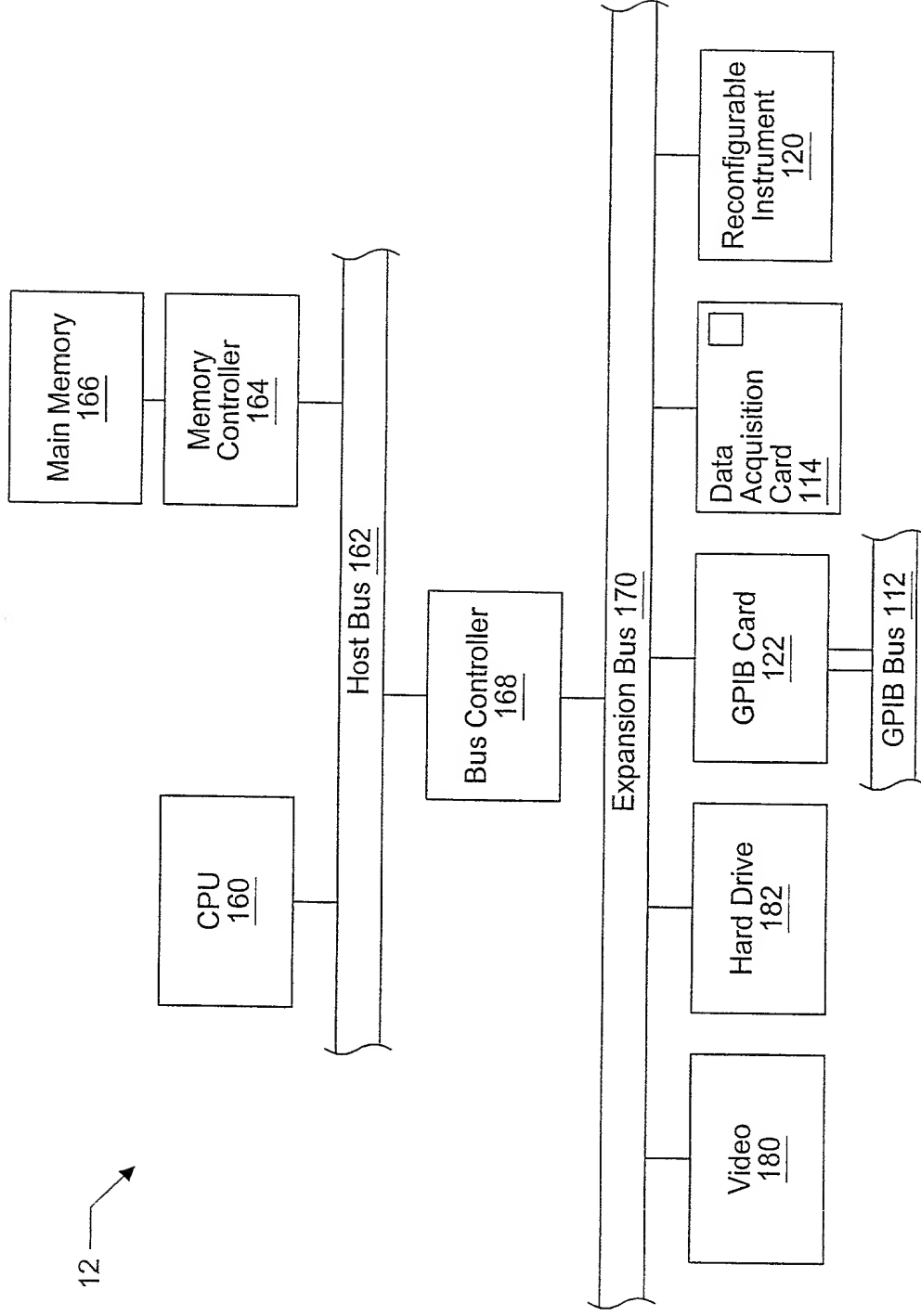


Figure 2

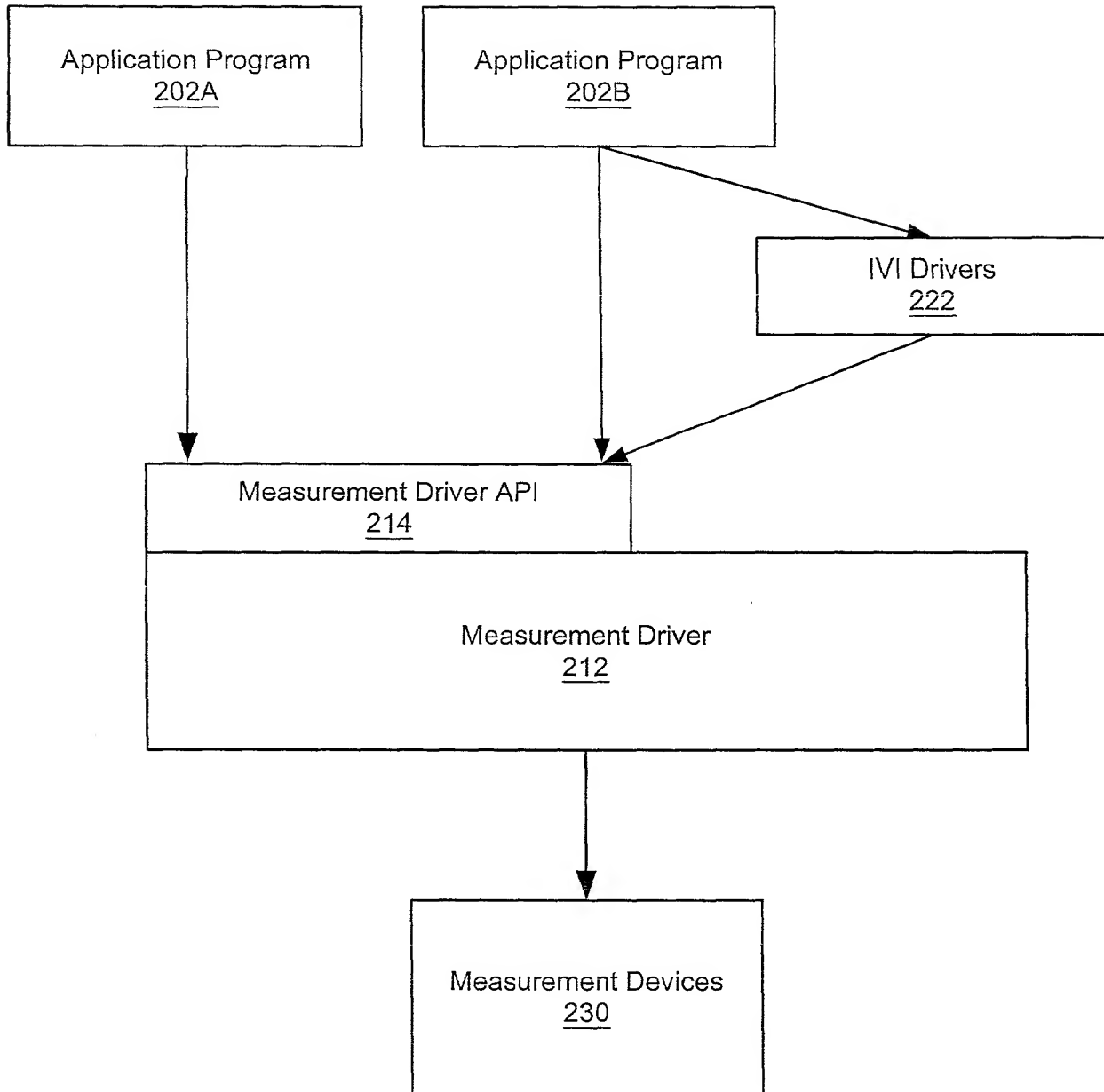


Figure 3

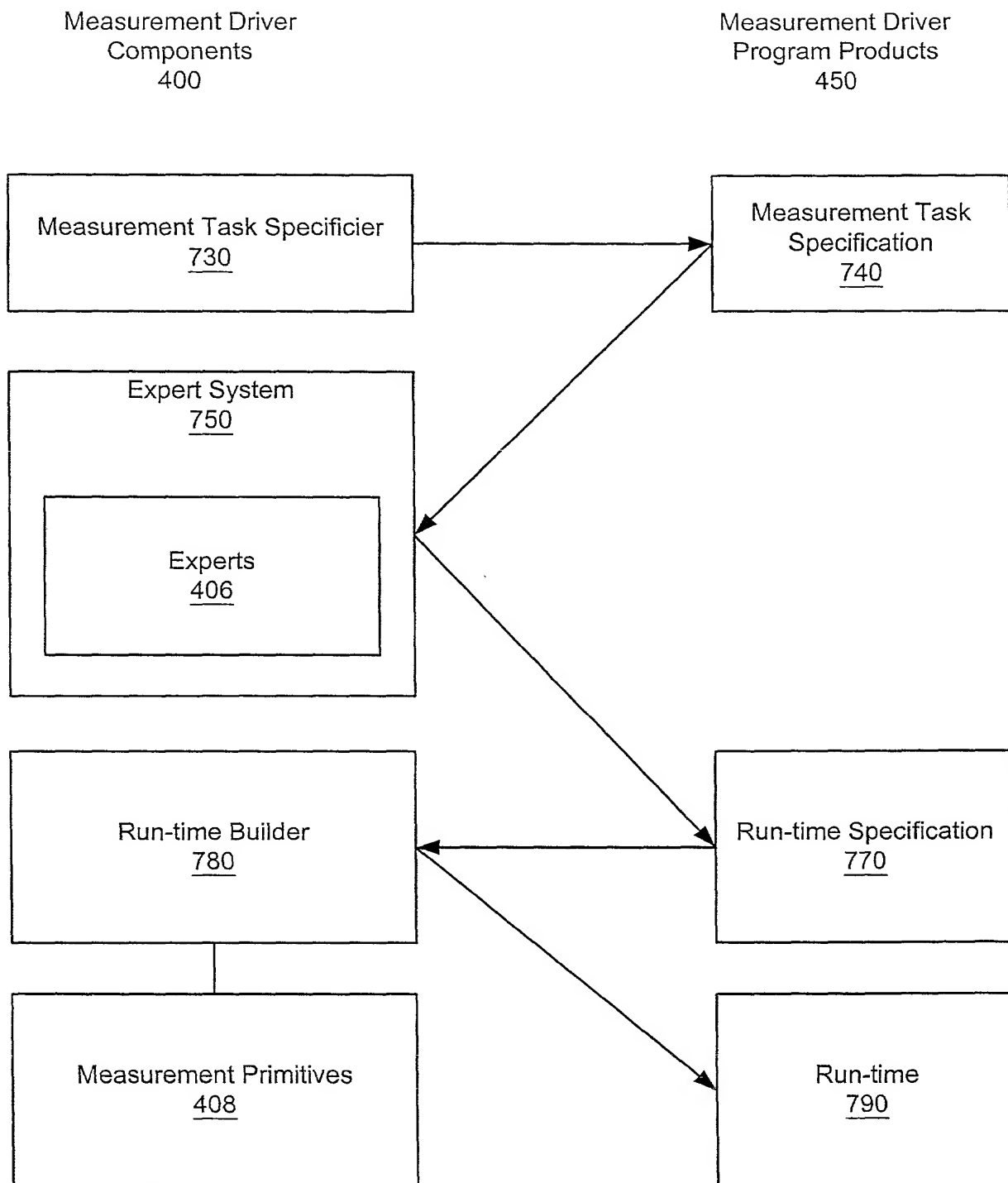


Figure 4

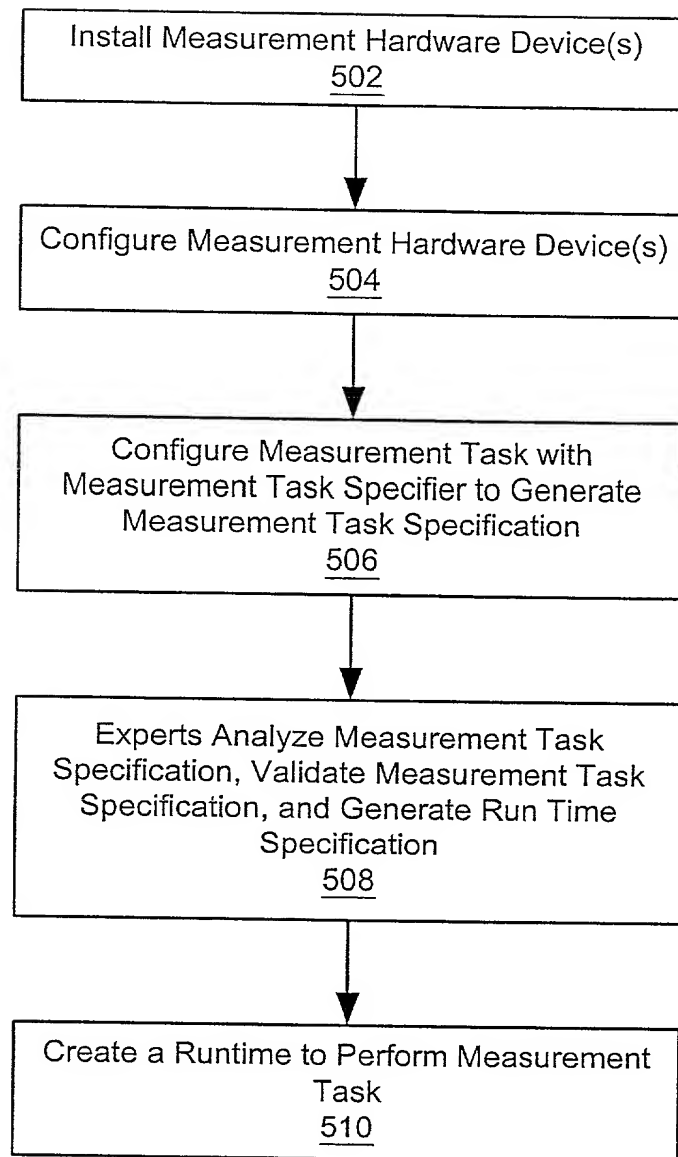
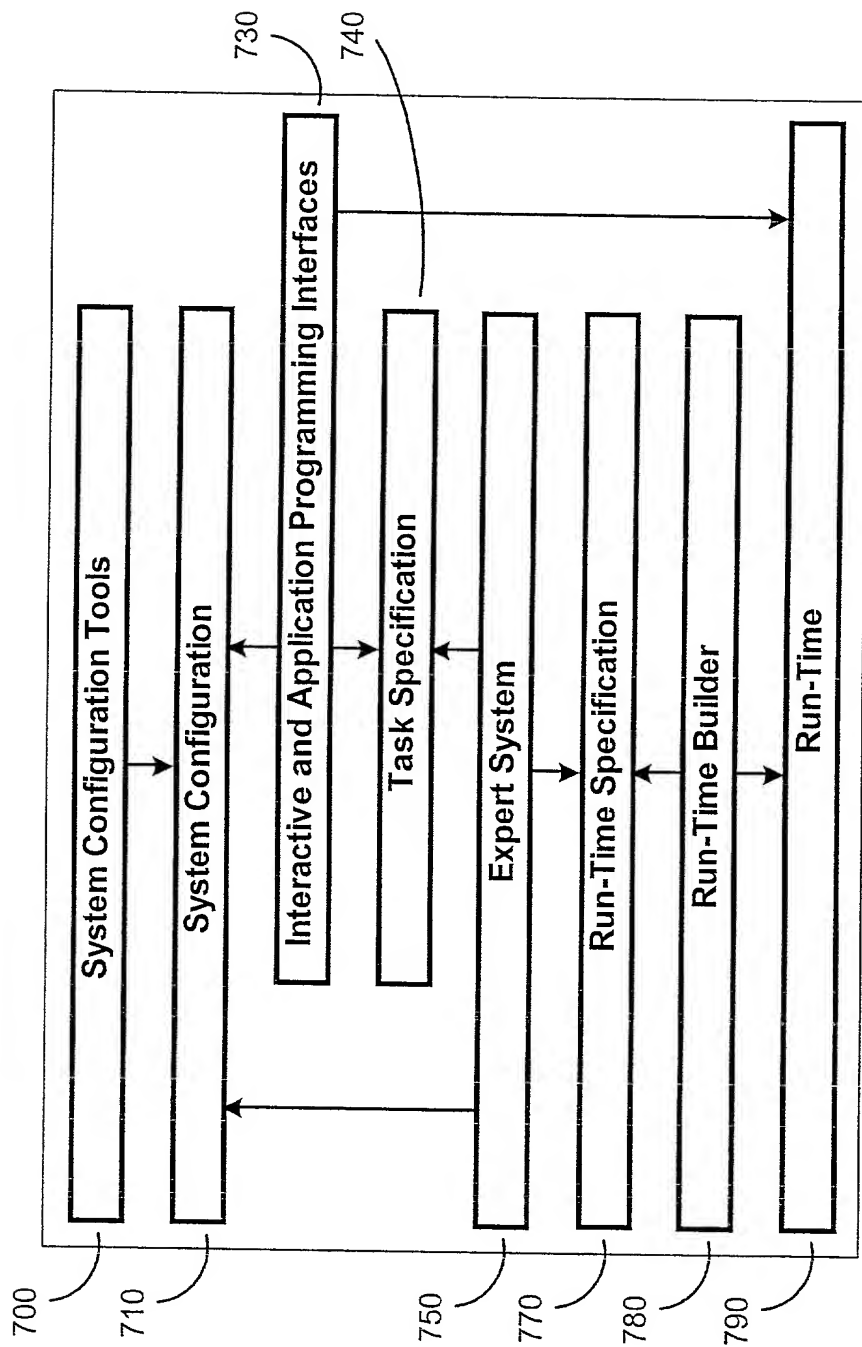


Figure 5



High-Level Architecture

Figure 6

System Configuration and Task Specification

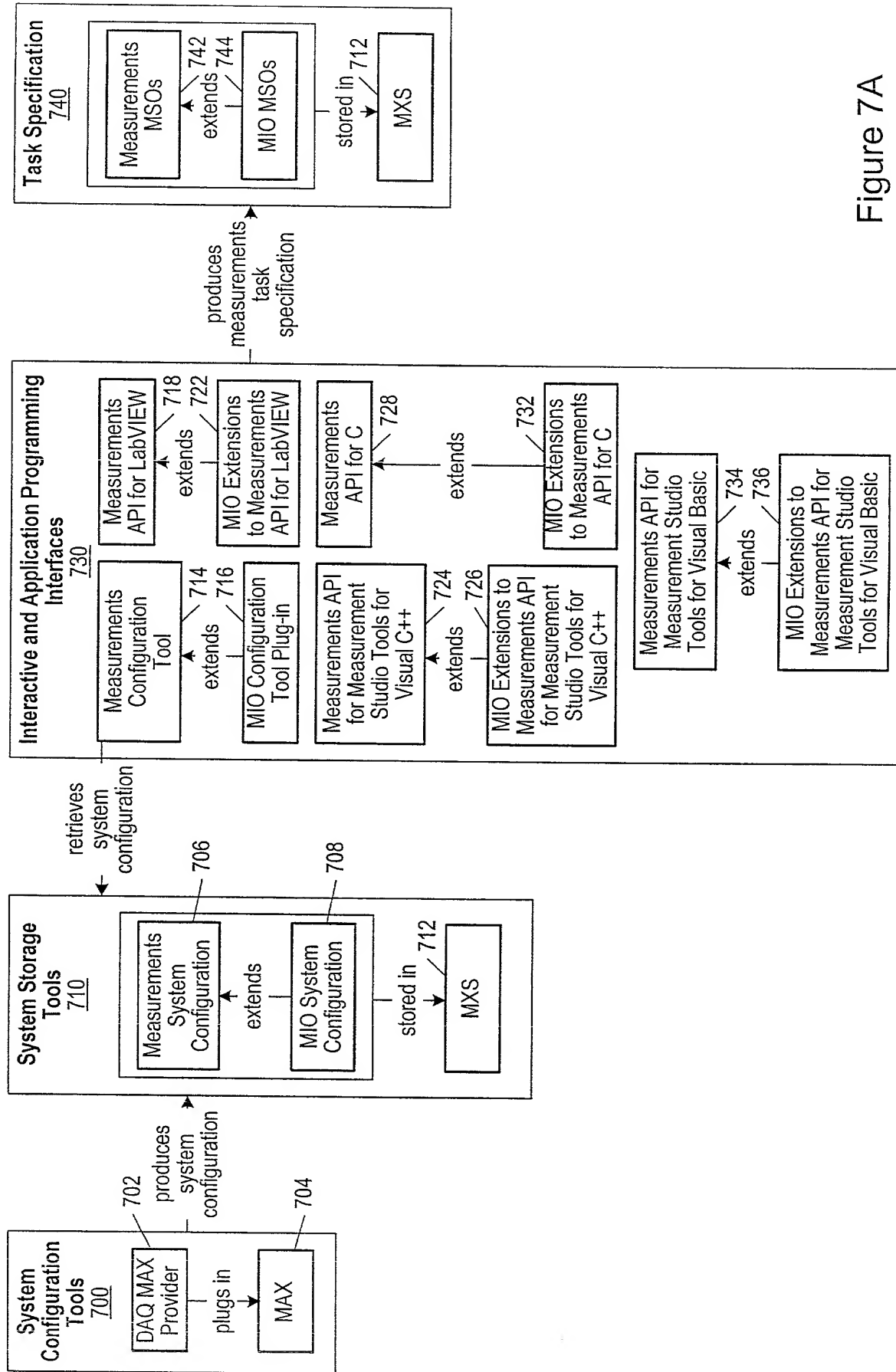


Figure 7A

Building Task Run-time from Task Run-time Specification

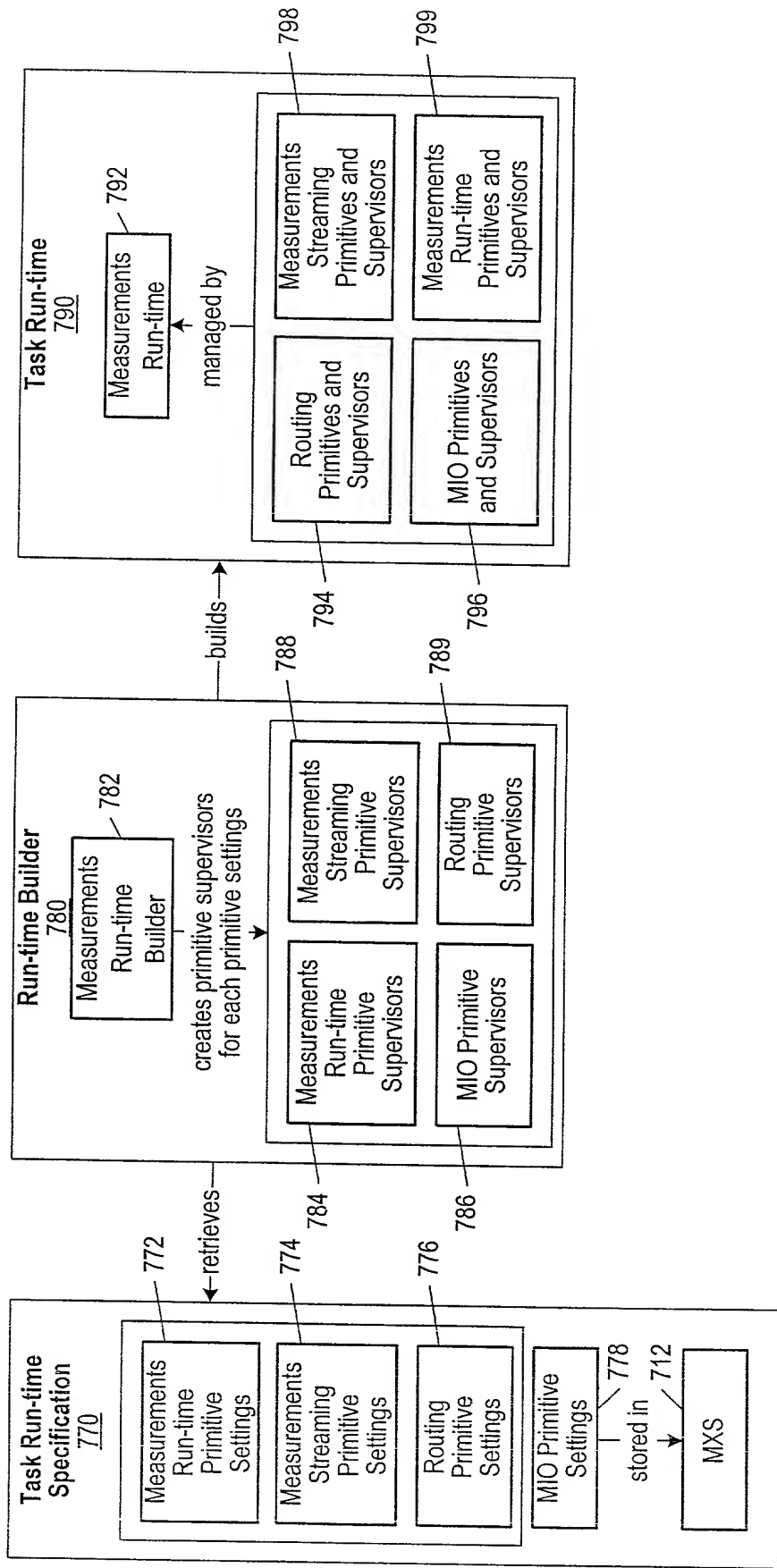


Figure 7C

Executing Tasks

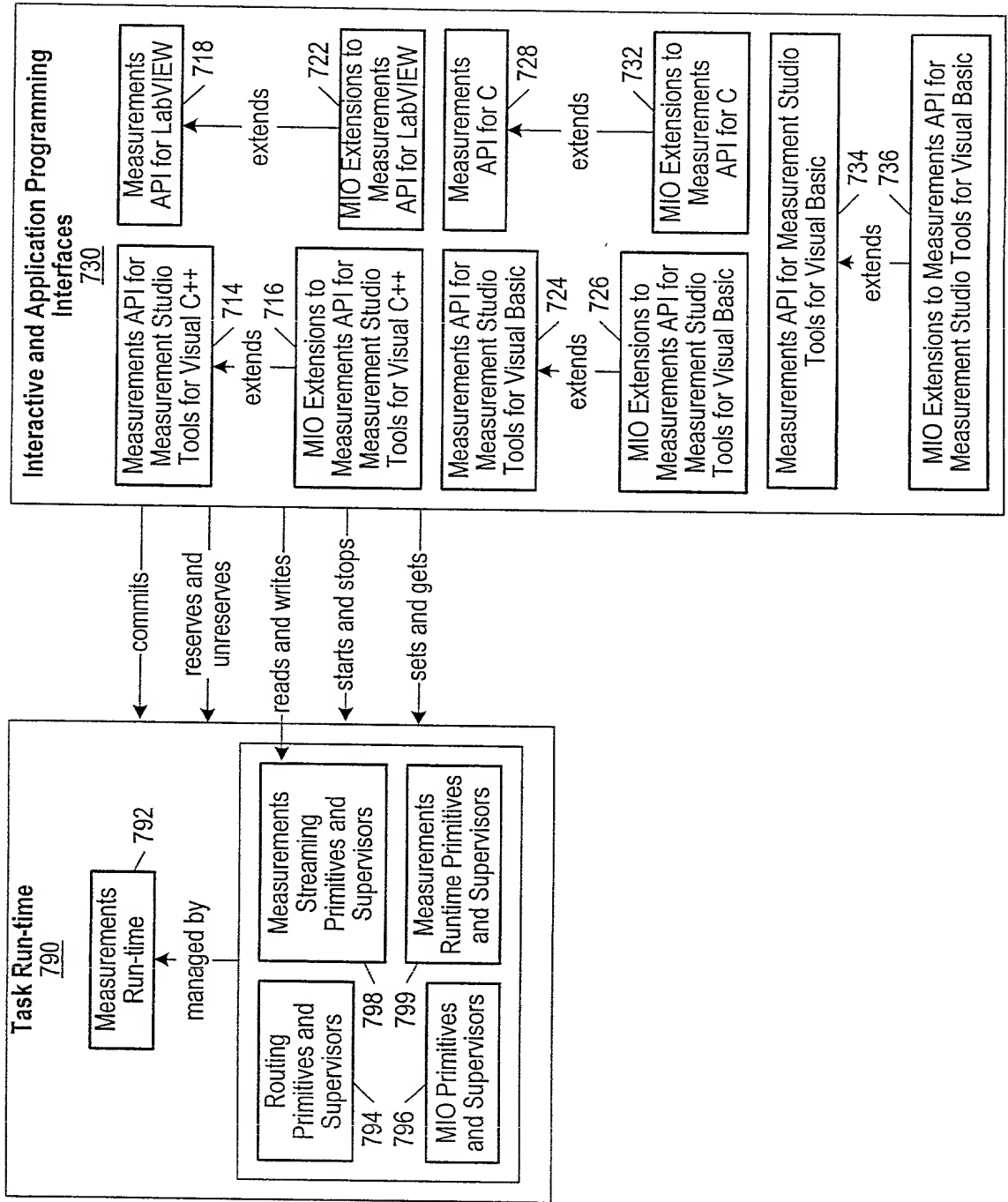


Figure 7D

Packages for System Configuration and Task Specification

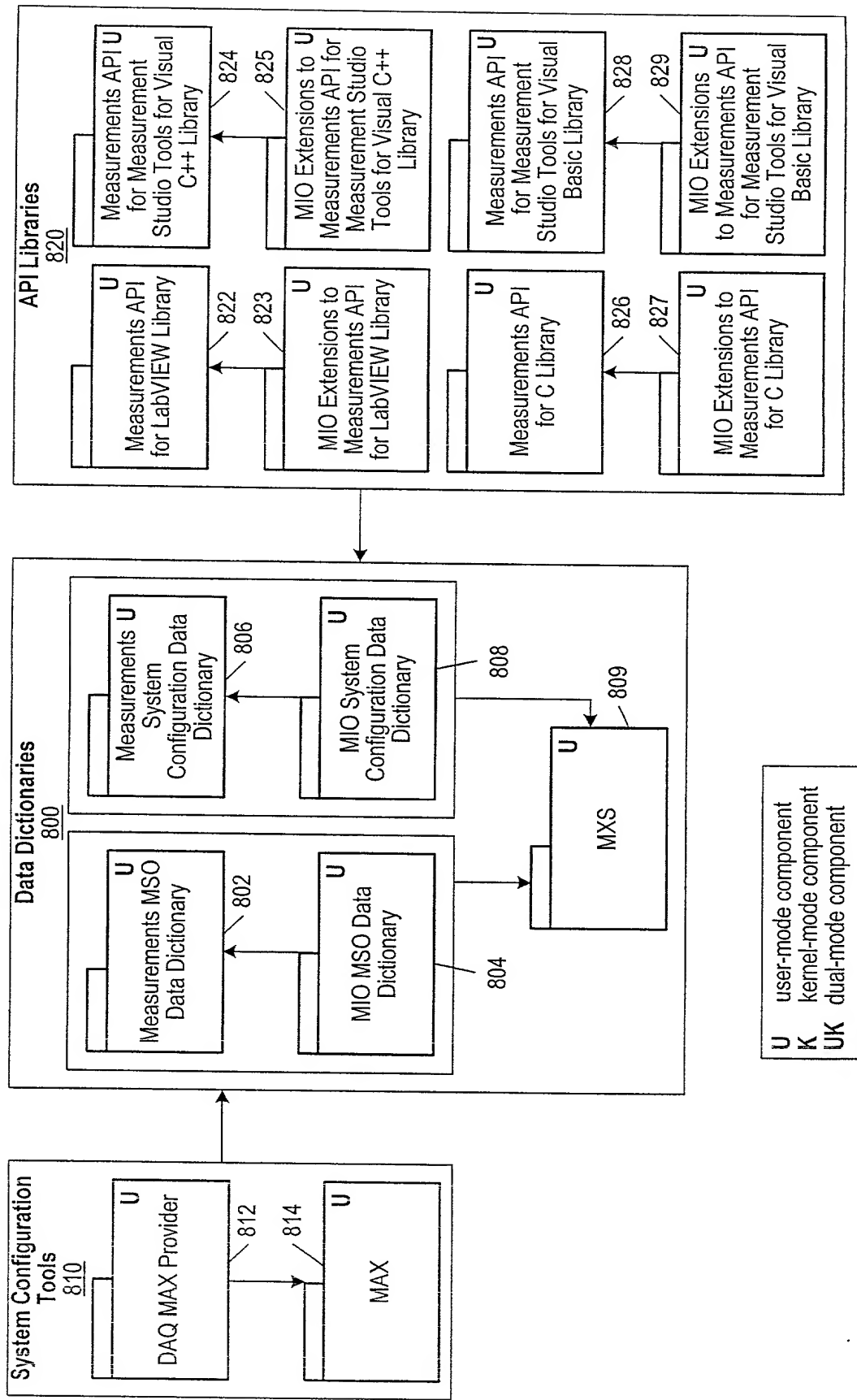


Figure 8A

Packages for Compiling Task Specification to Run-time Specification

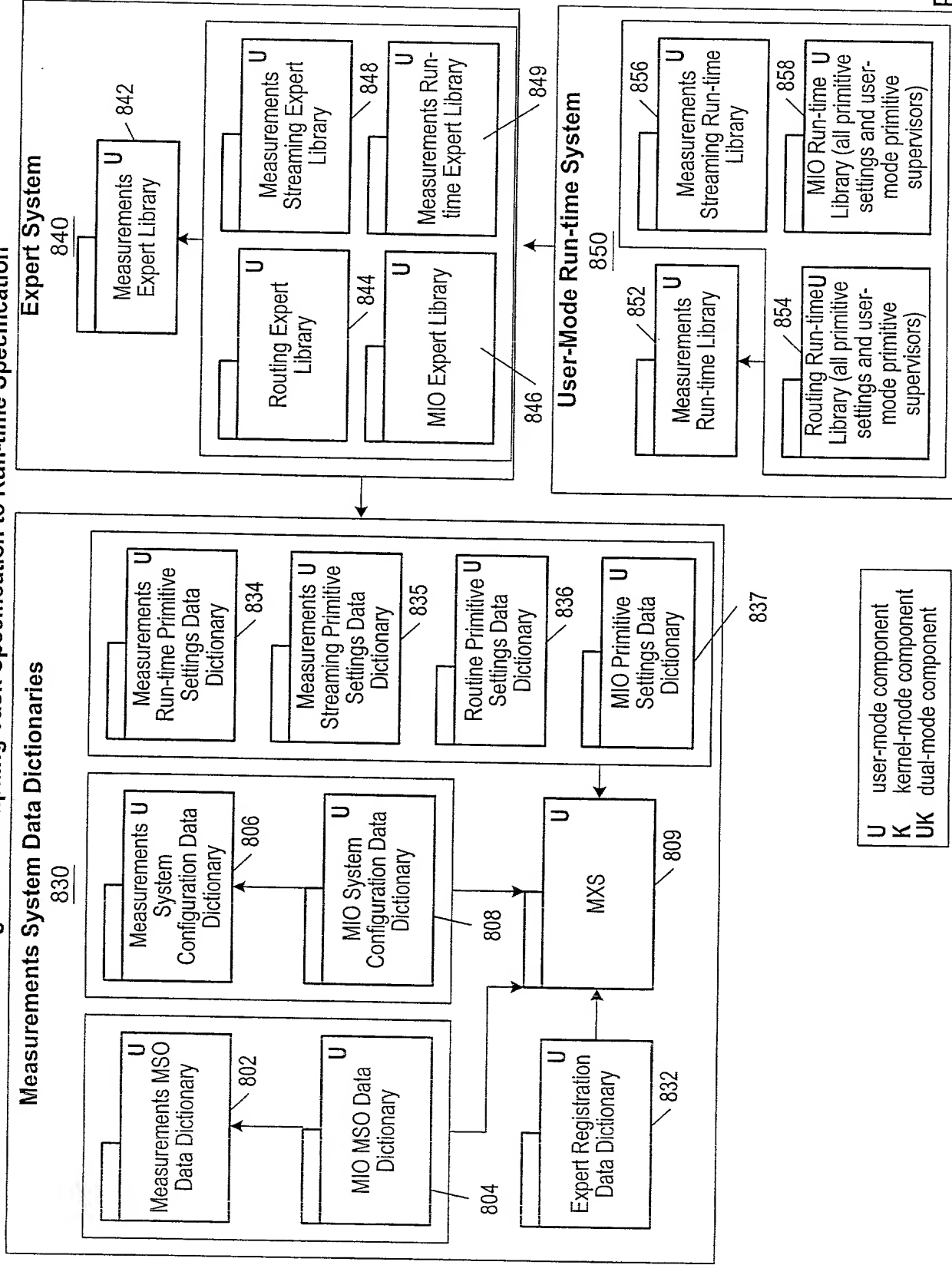


Figure 8B

Packages for Building Task Run-time from Run-time Specification

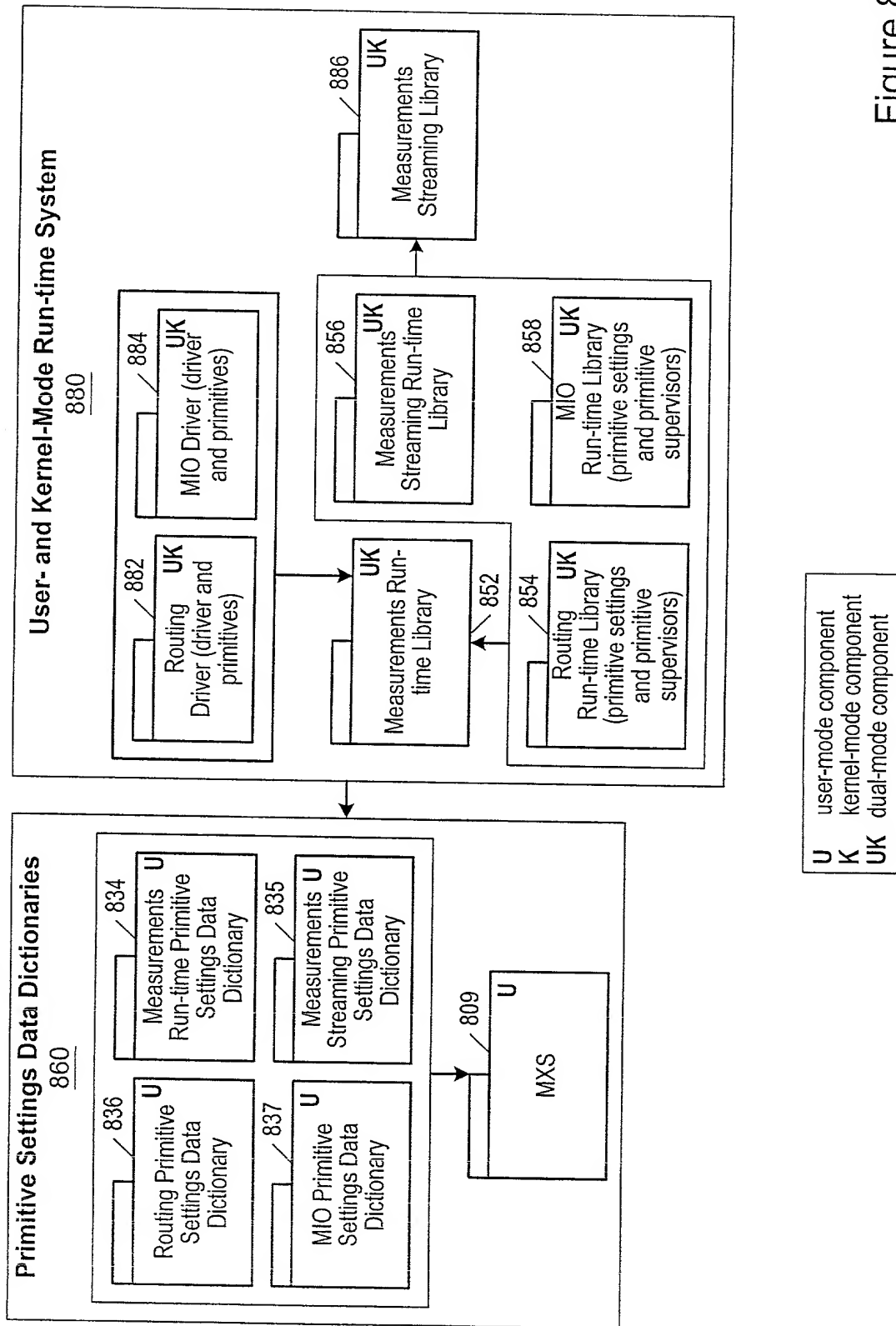


Figure 8C

Packages for Executing Task Run-time

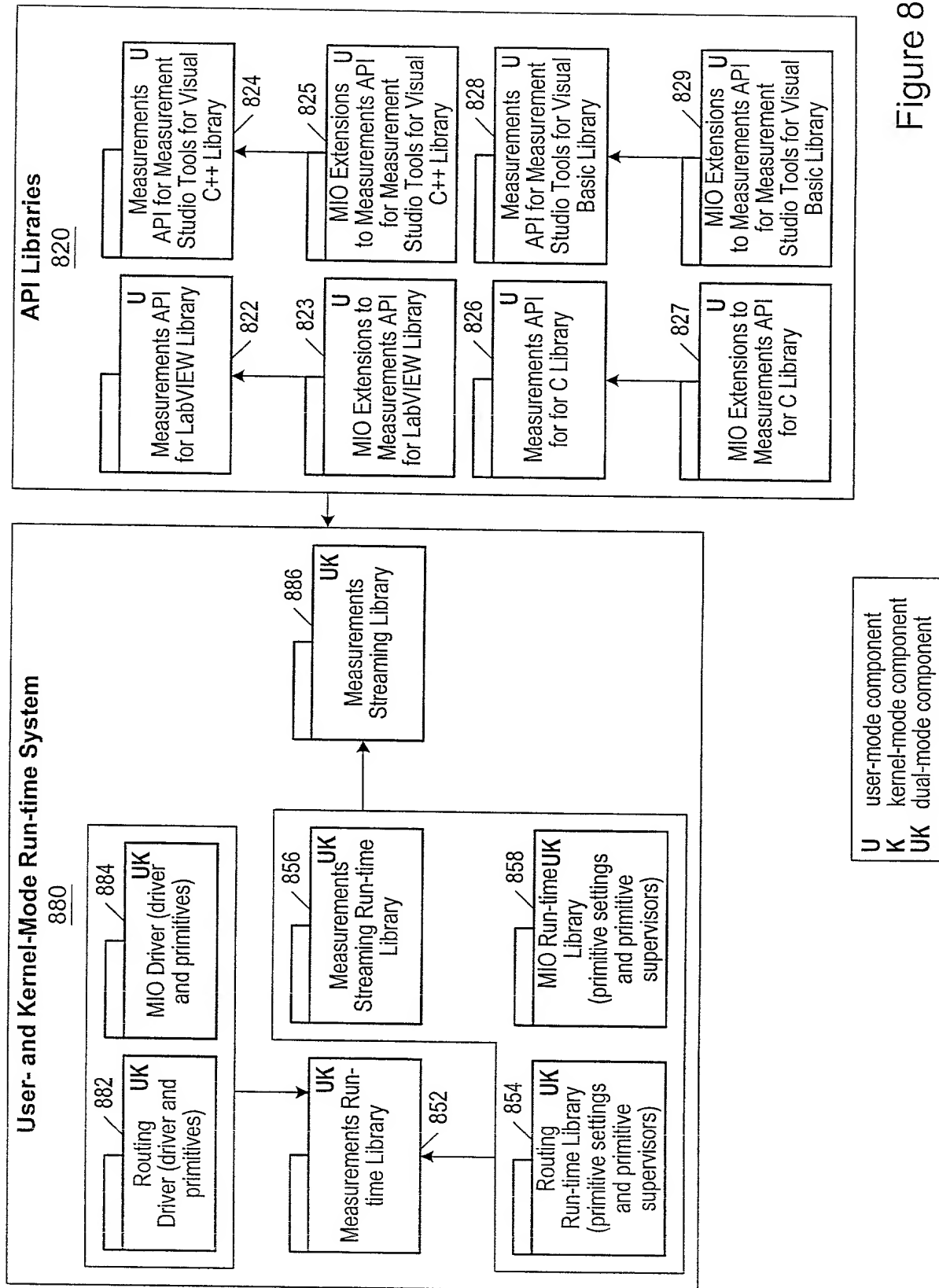


Figure 8D

State Diagram for Measurement Tasks

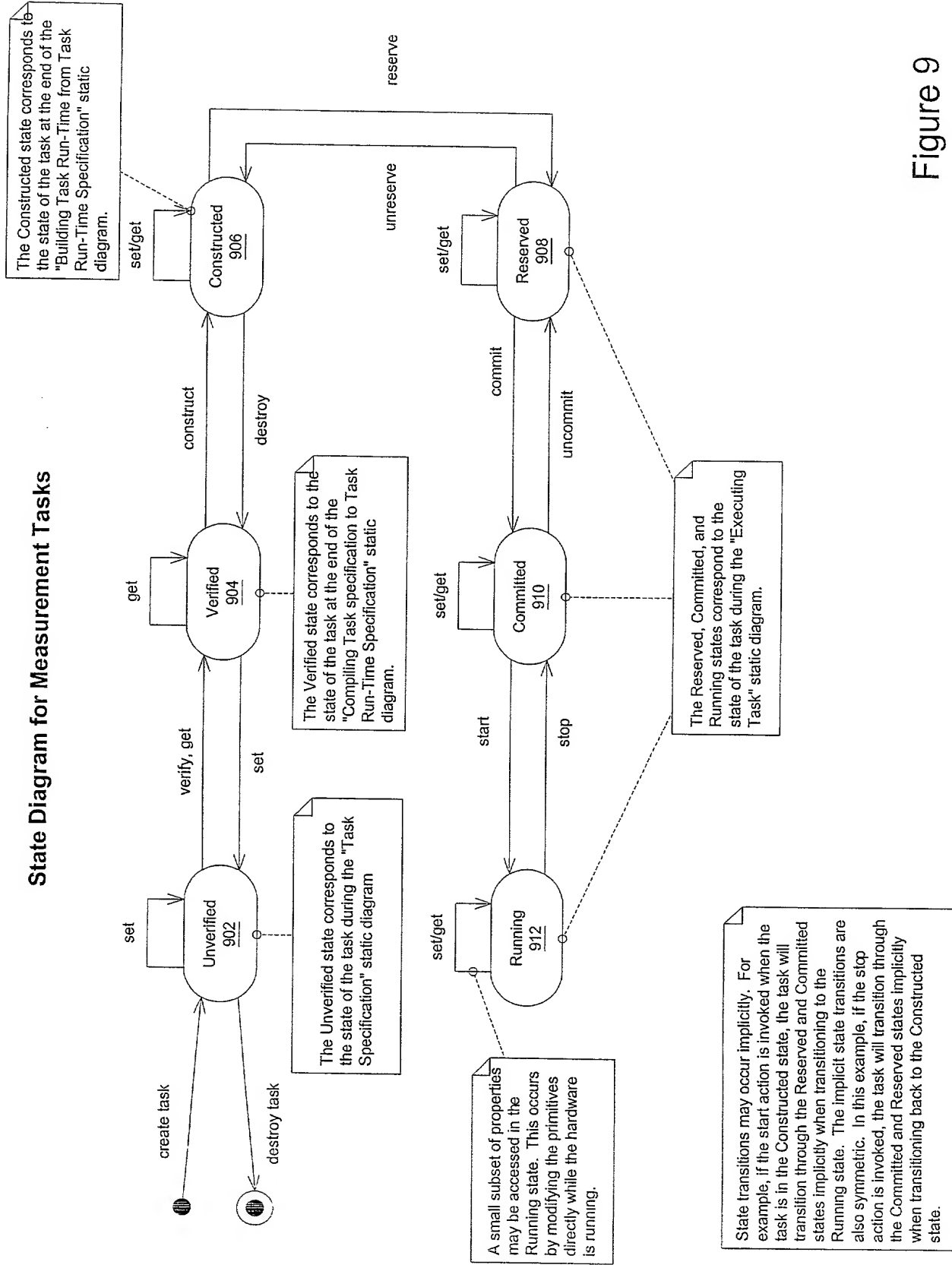


Figure 9

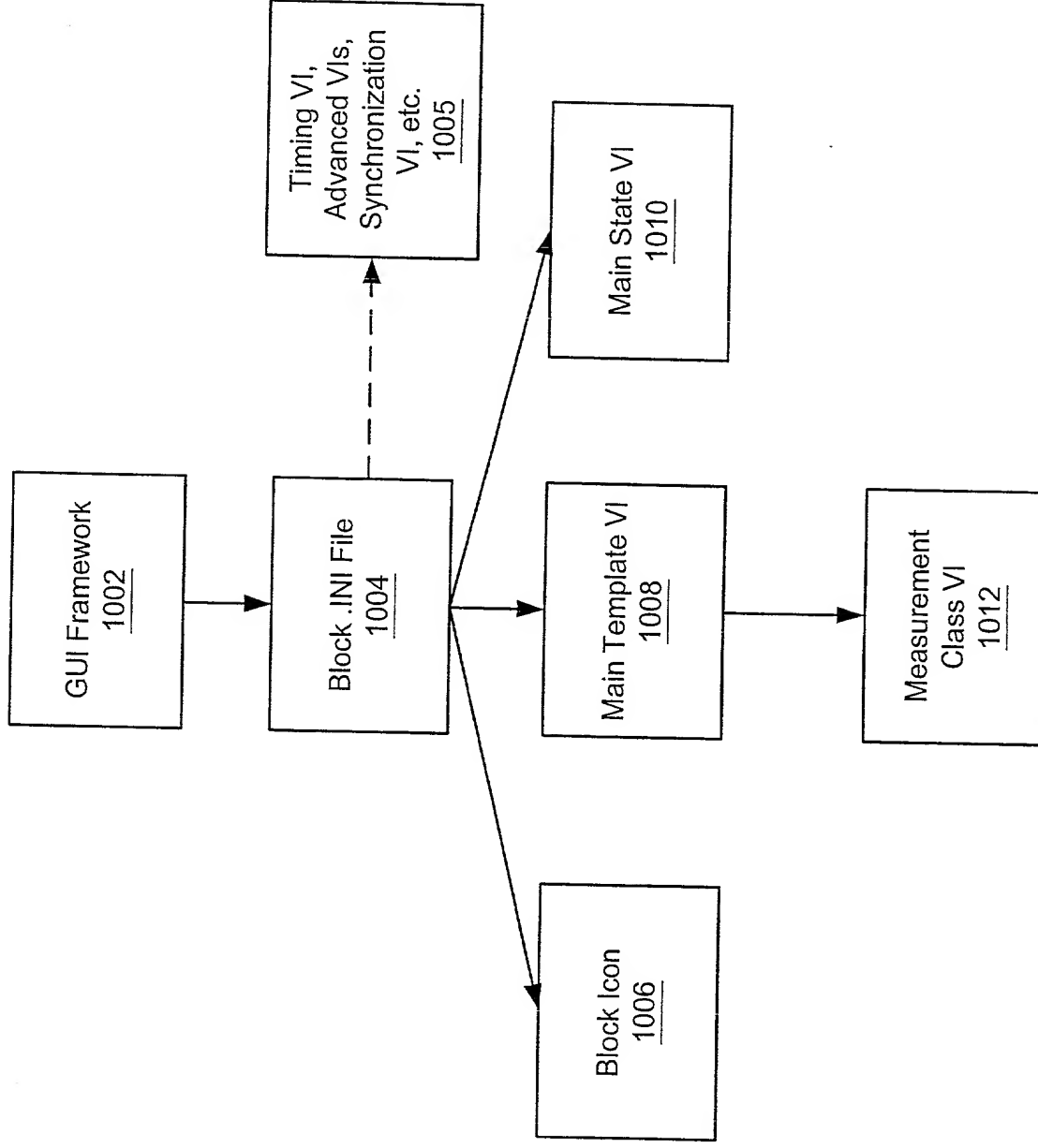


Figure 10

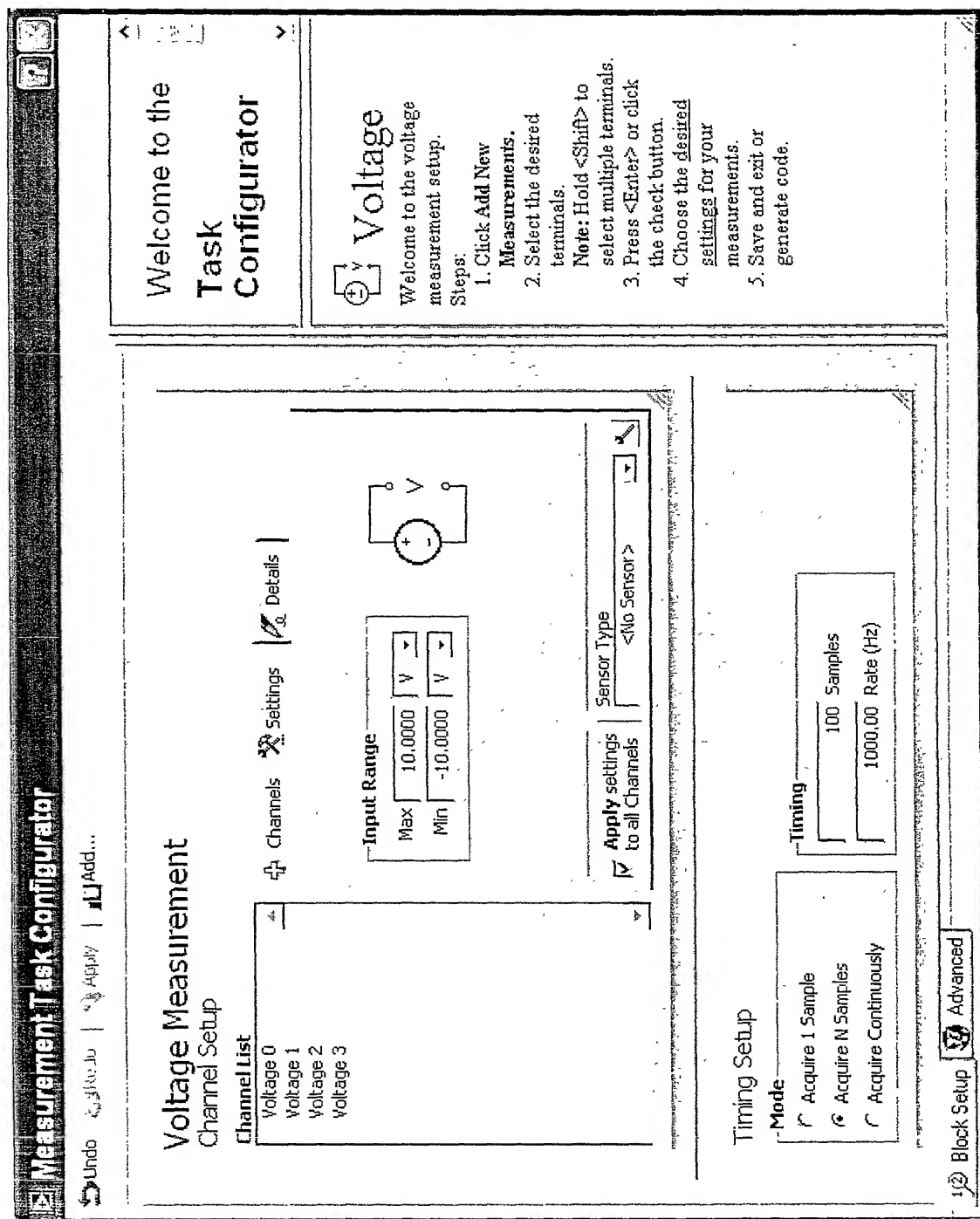


Figure 11

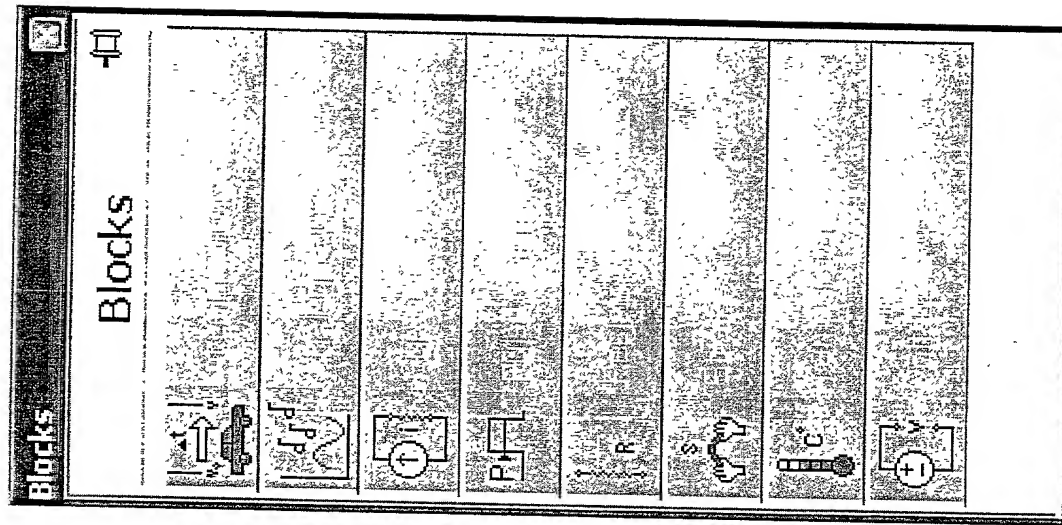


Figure 12A

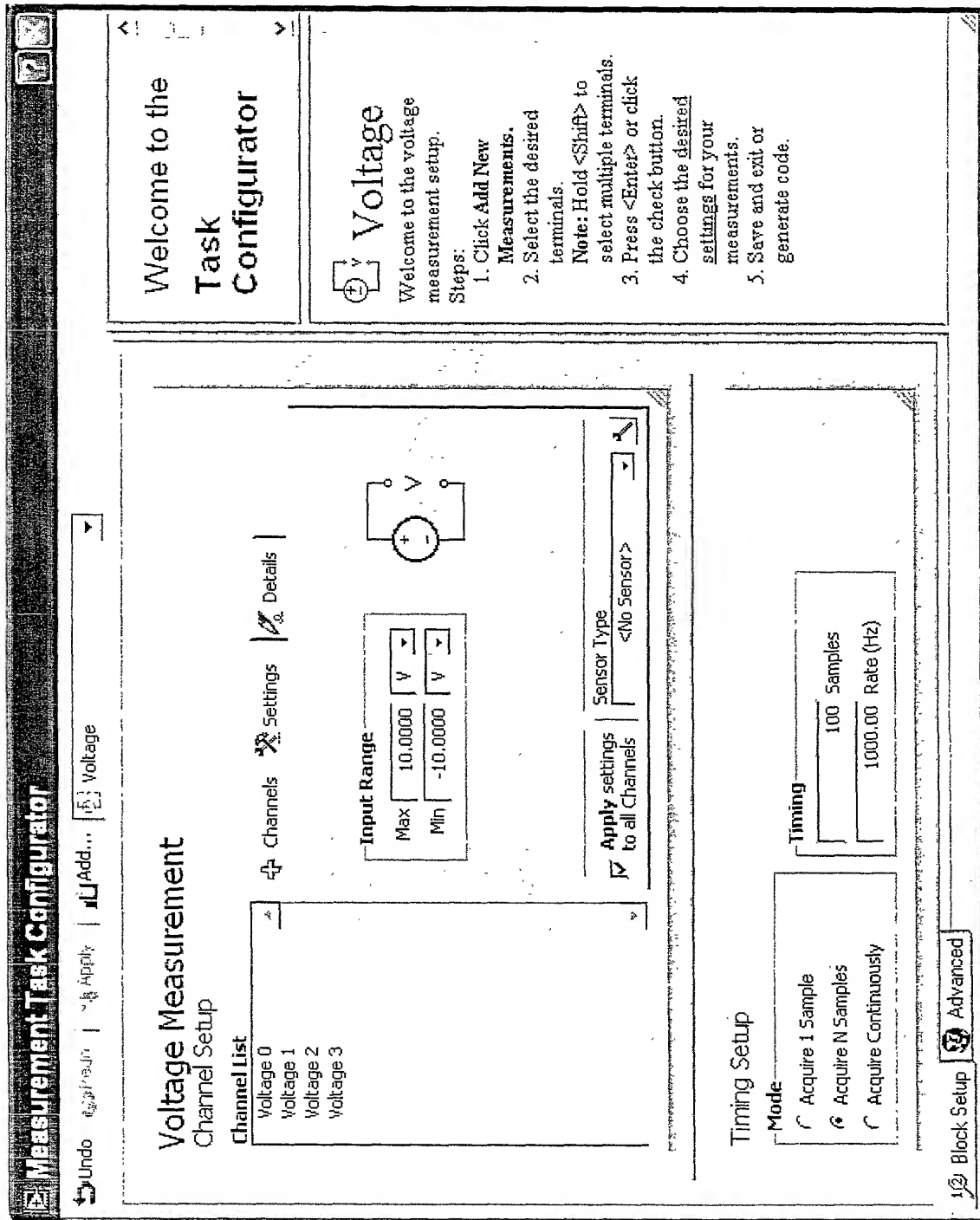


Figure 12B

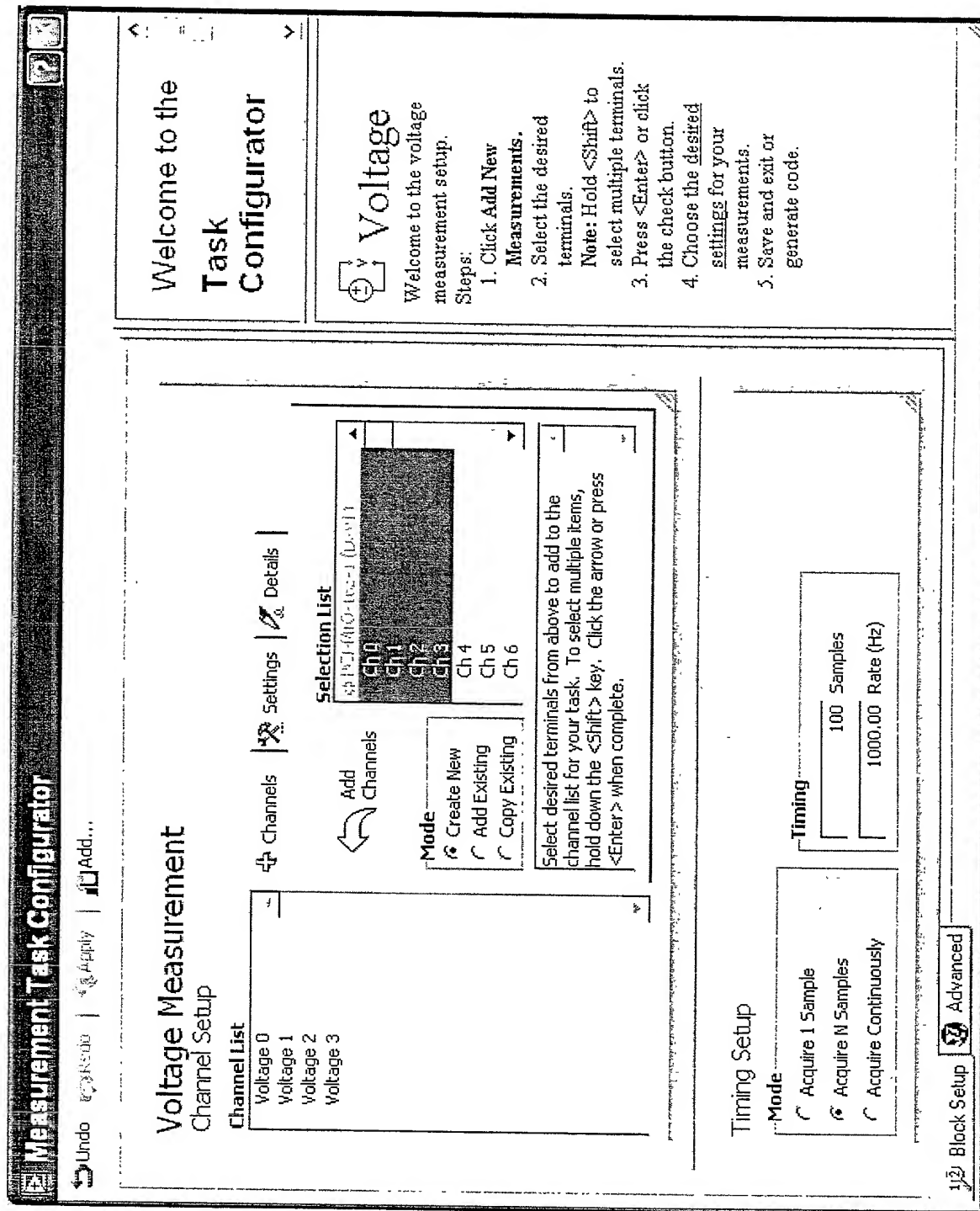


Figure 12C

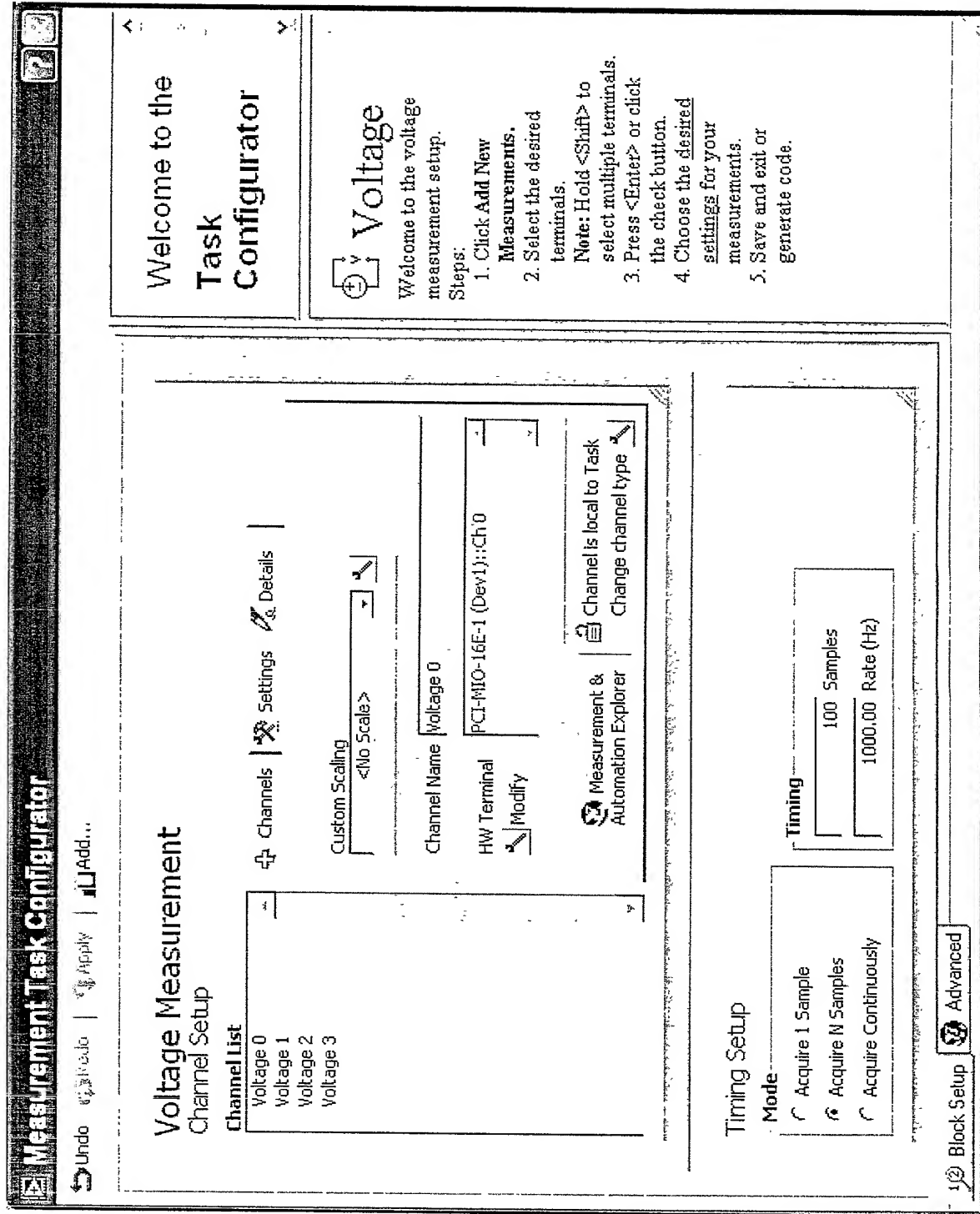


Figure 12D

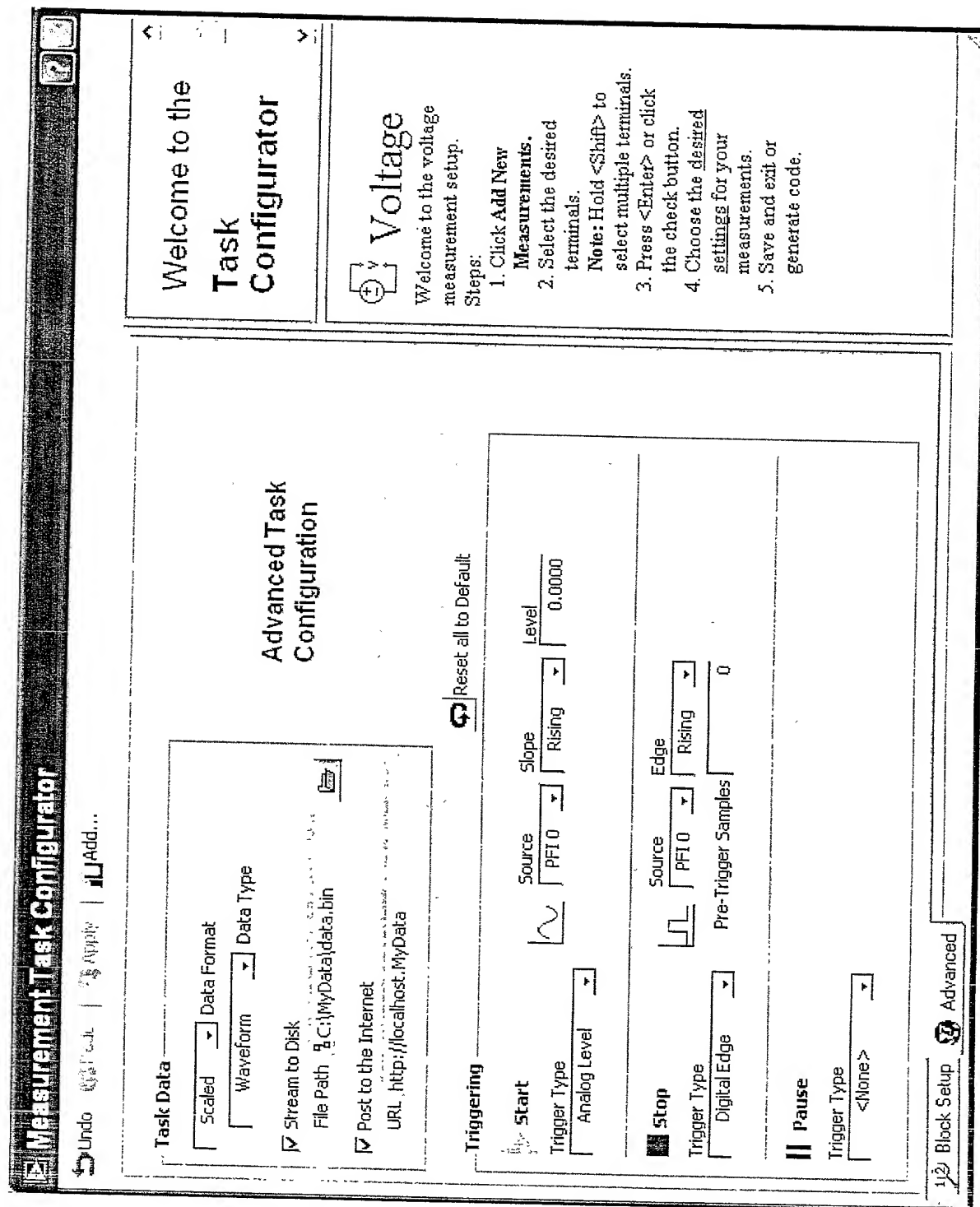


Figure 13

Figure 14

10010396-11304

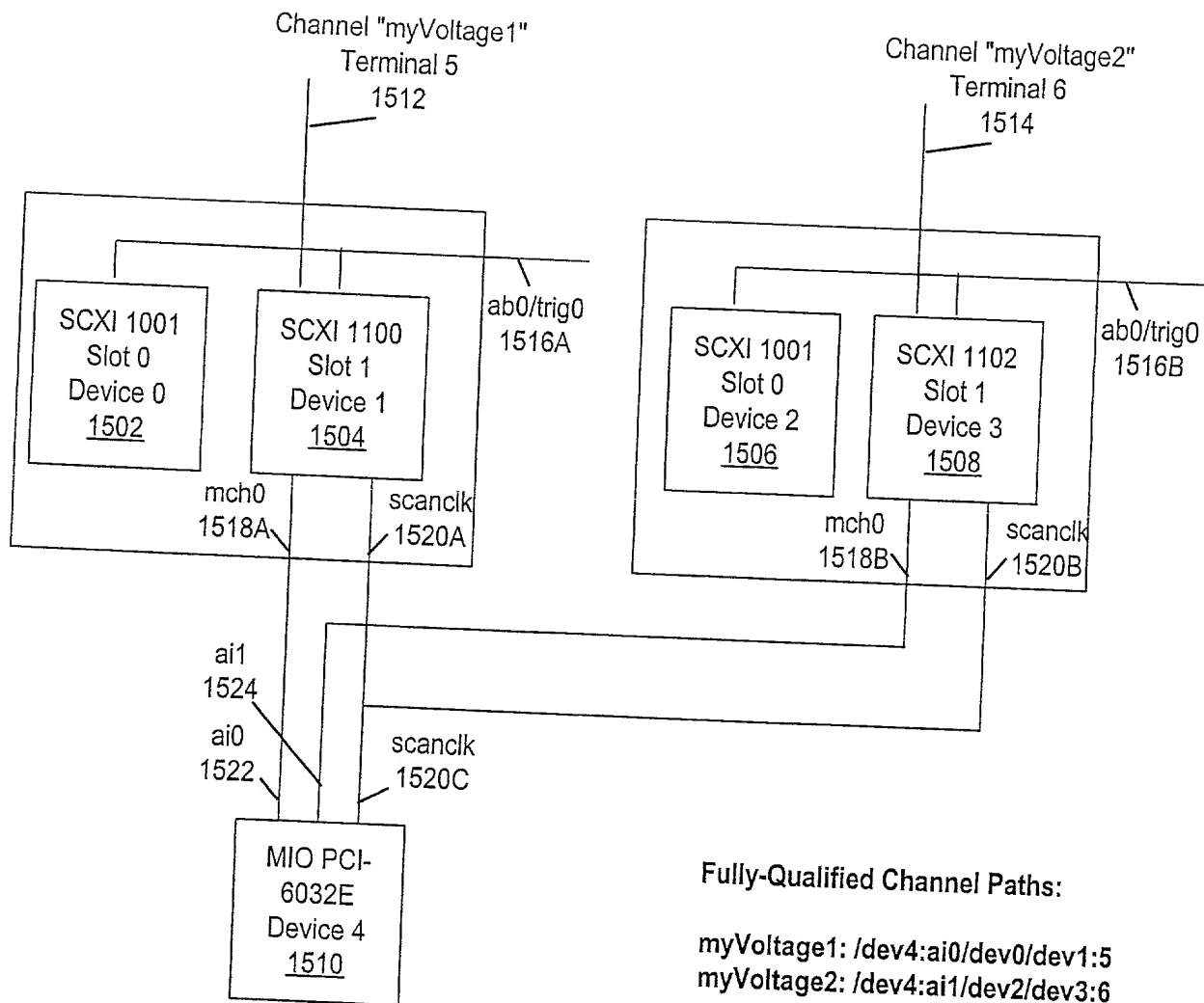
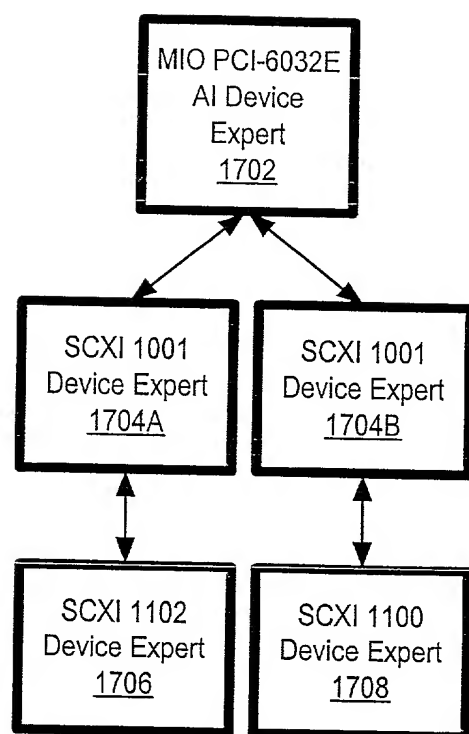


Figure 15

[illegible]

Create Device Expert Call Tree

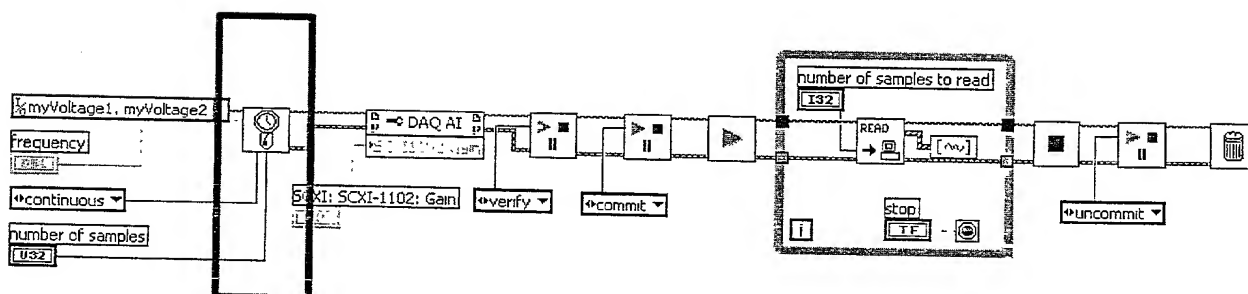
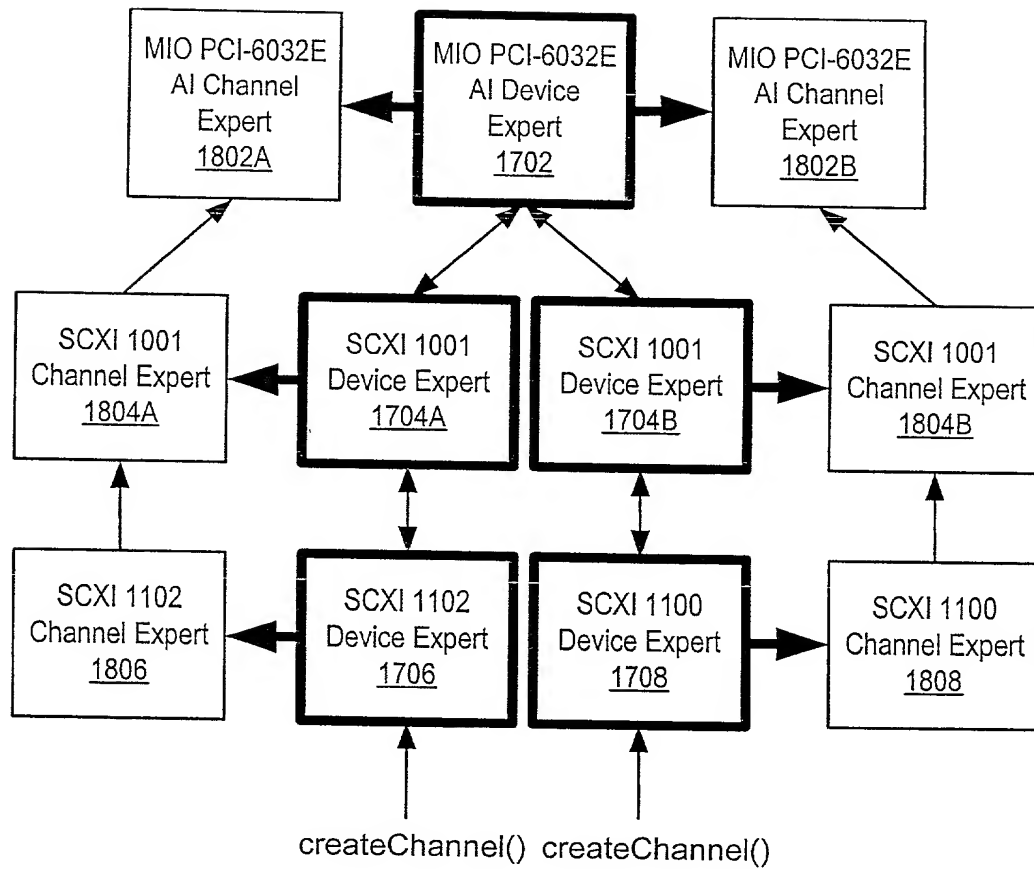


Figure 17



Create Channel Experts

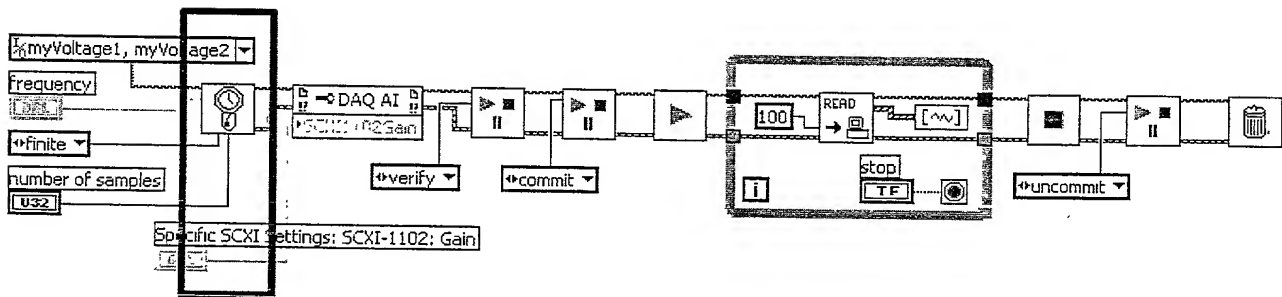


Figure 18

Deserialize Named Channel MSOs

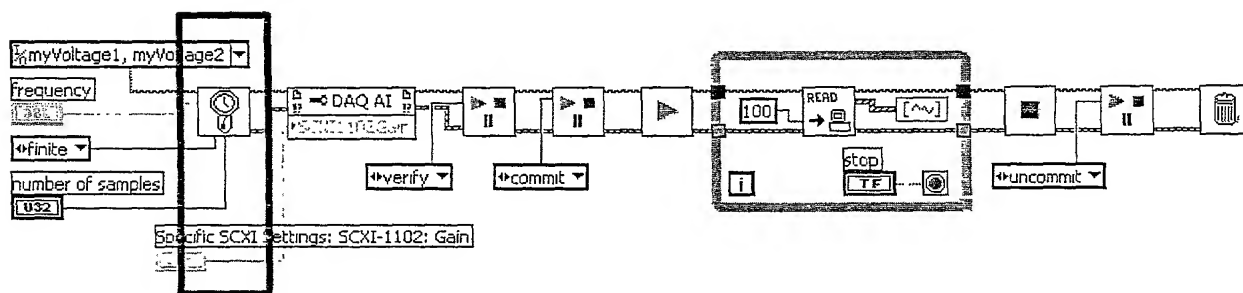
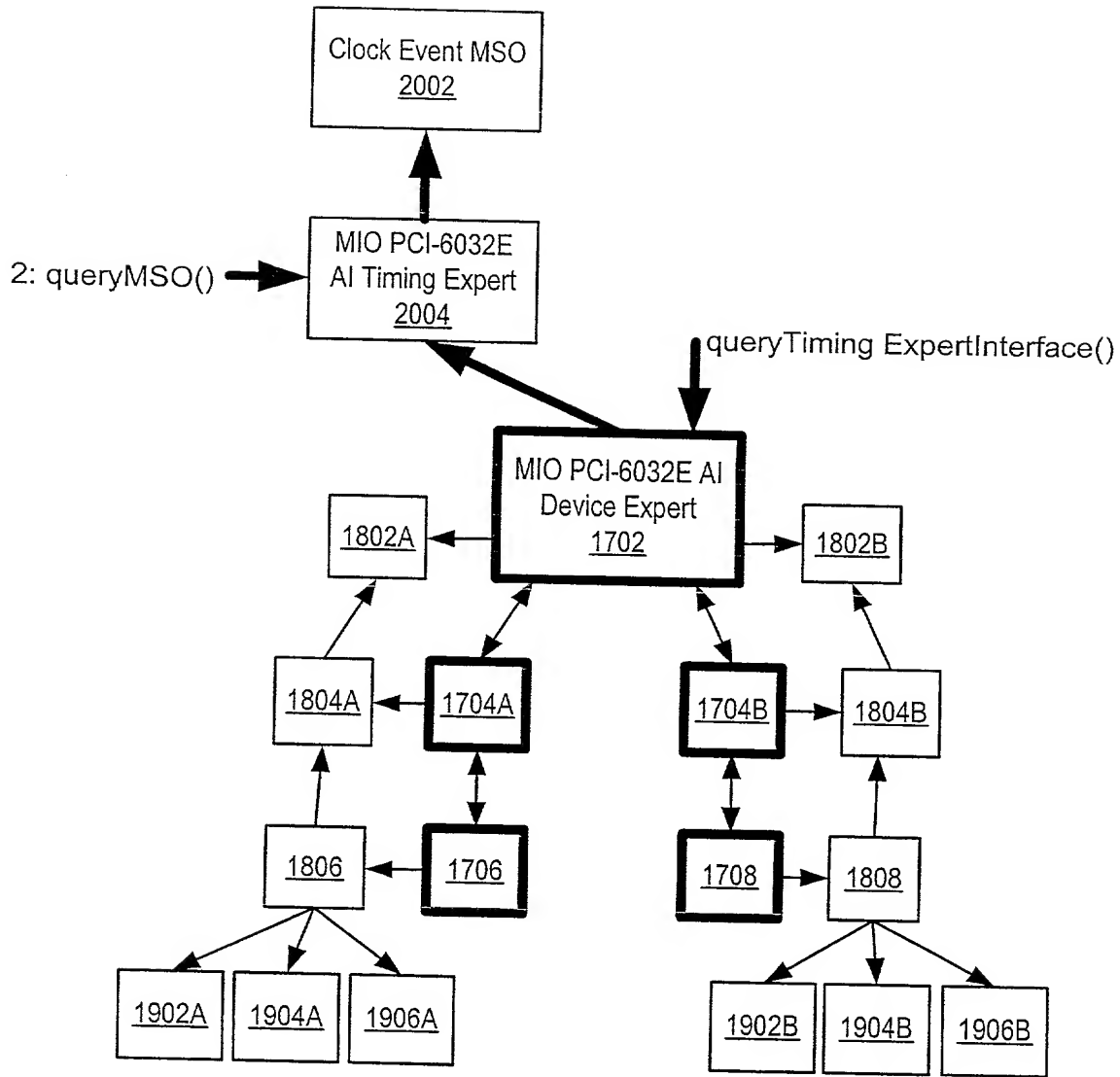


Figure 19



Configure Timing Experts

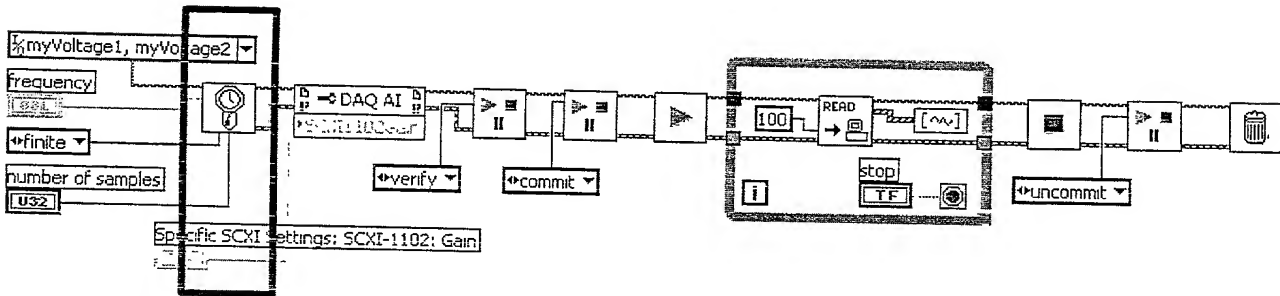
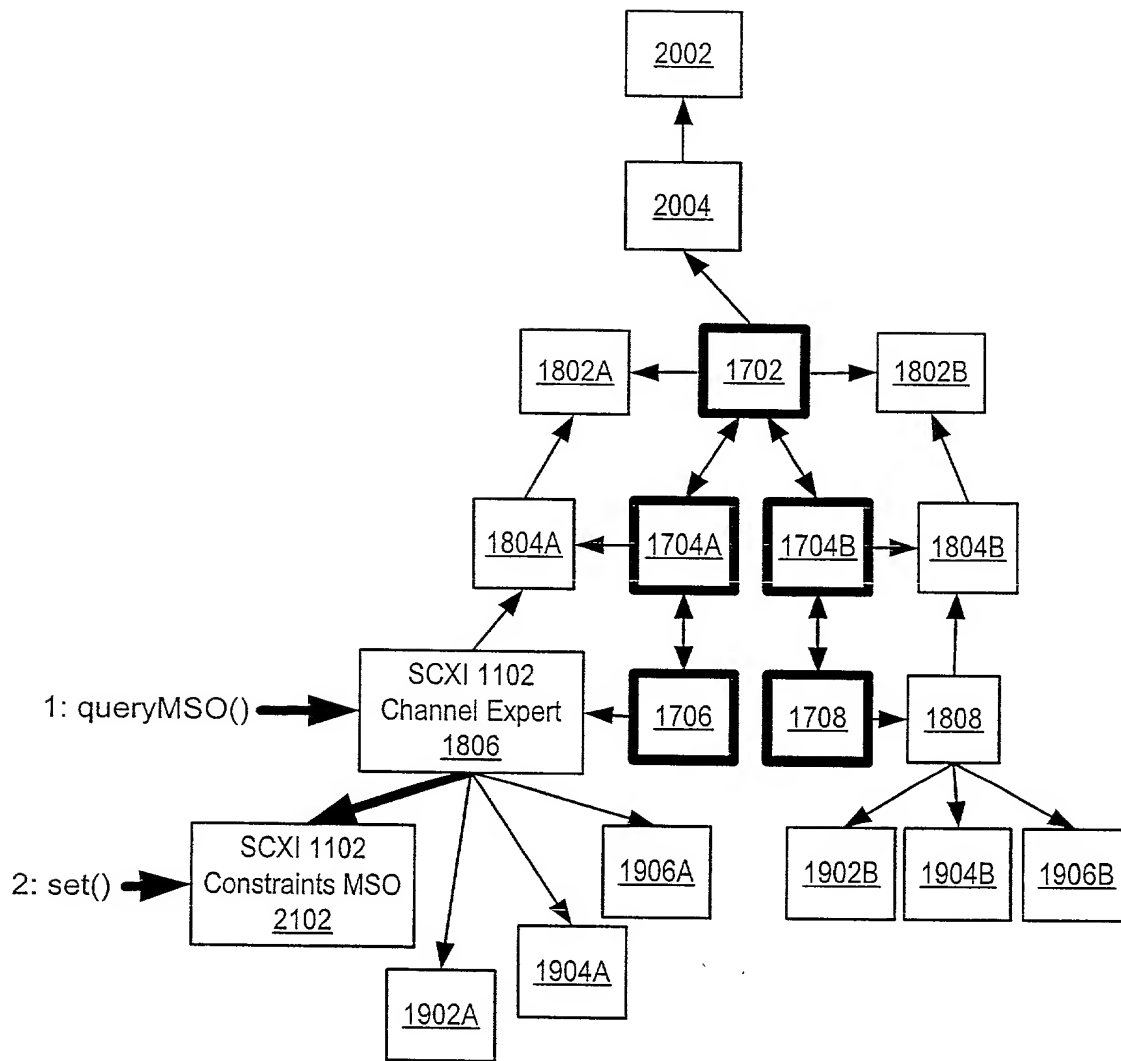


Figure 20



MSO Set Calls

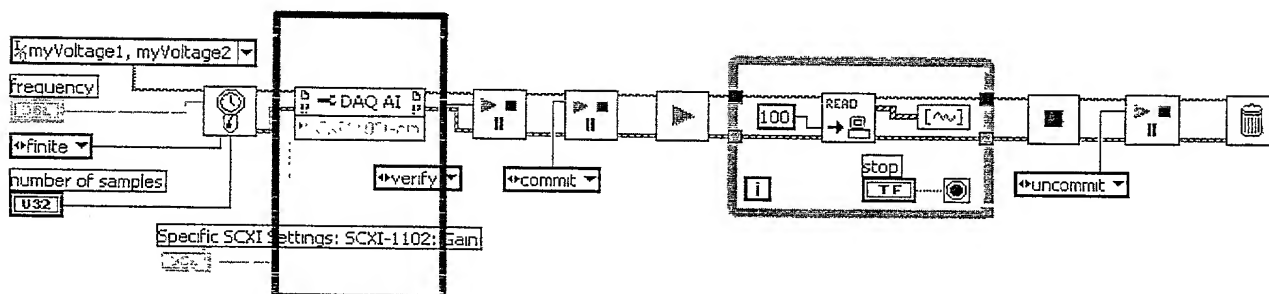
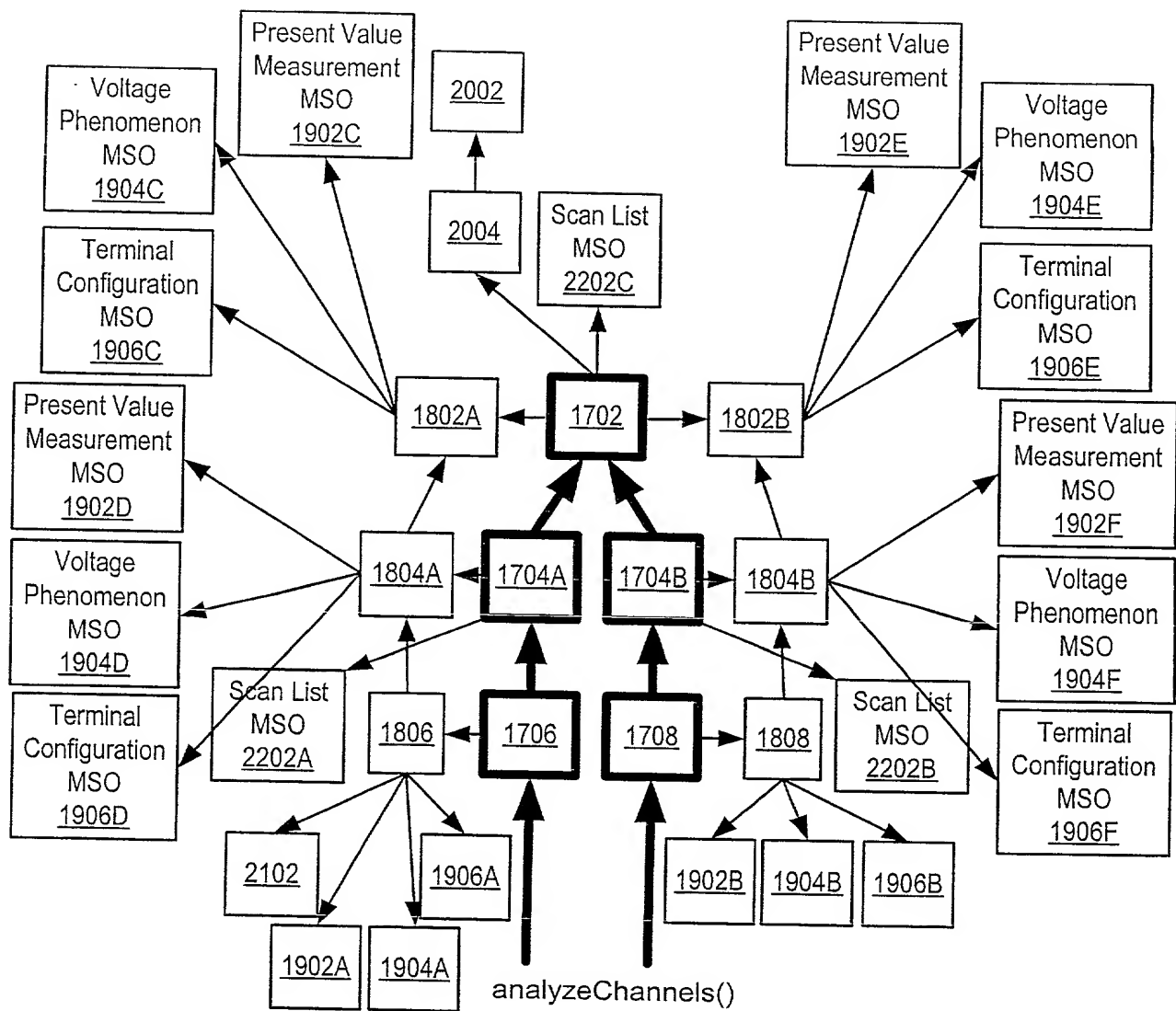


Figure 21



Analyze Channels

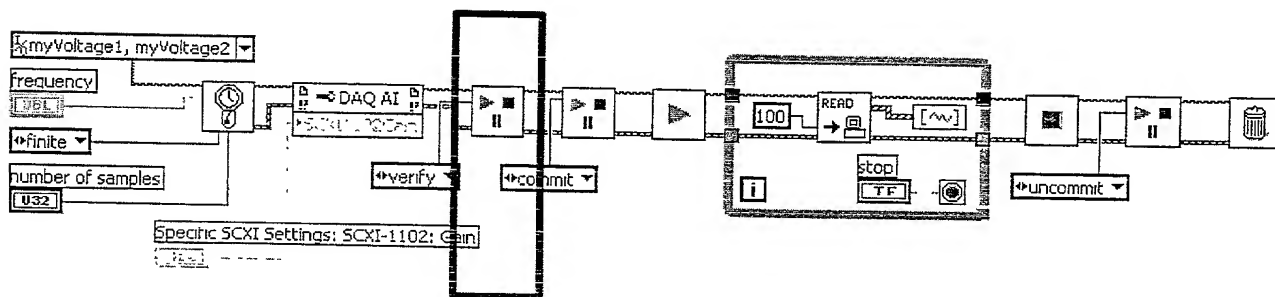
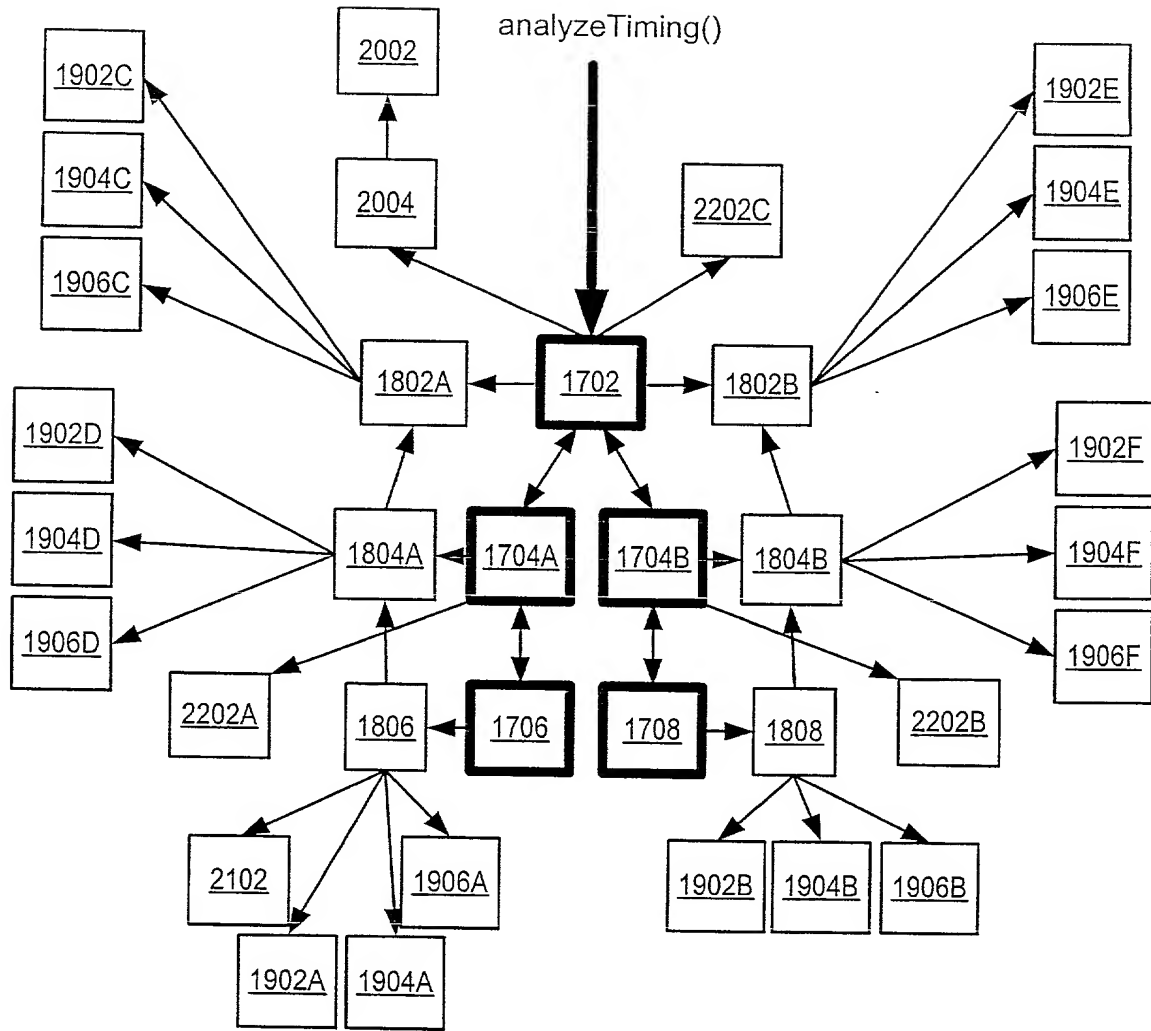


Figure 22



Analyze Timing

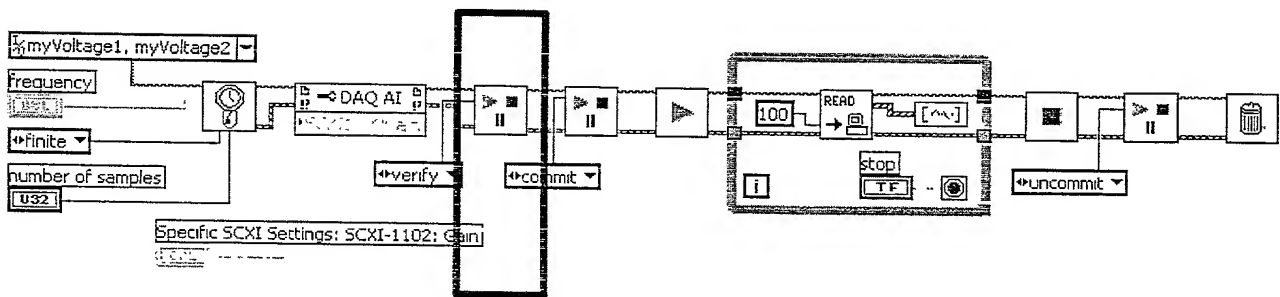
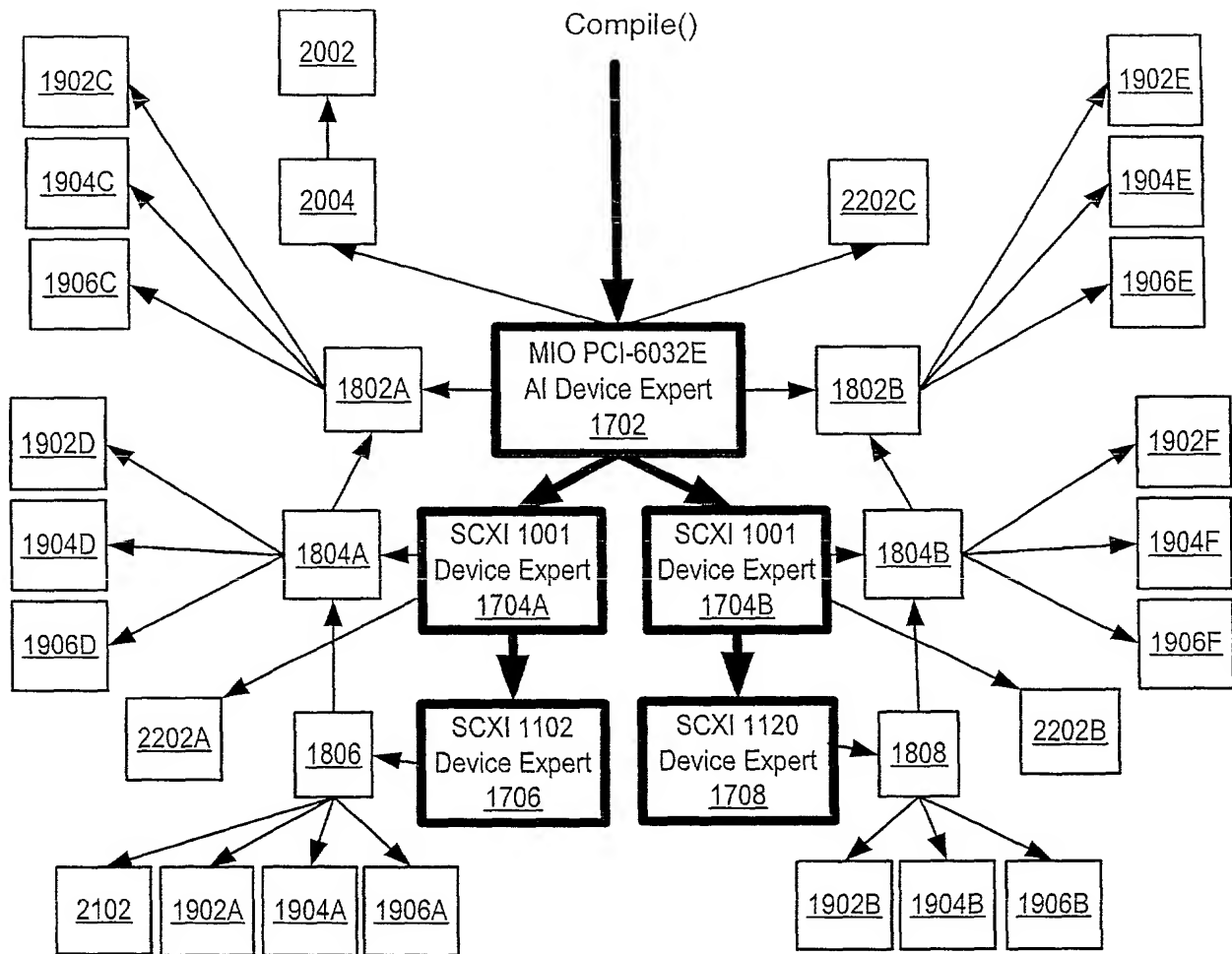


Figure 23



Compile

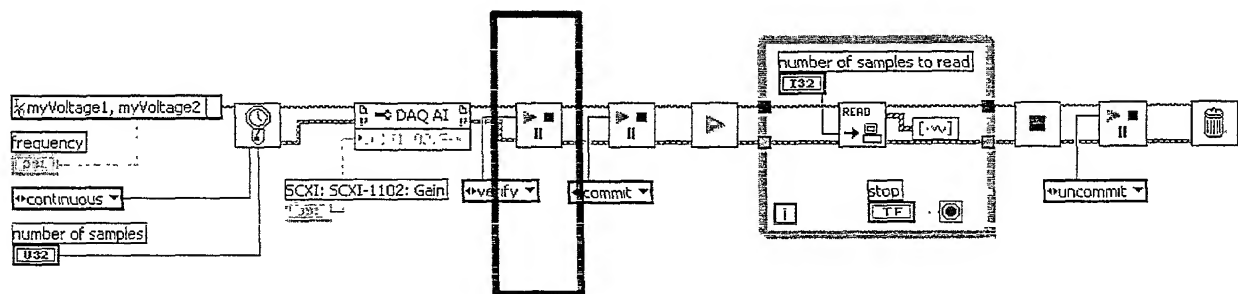
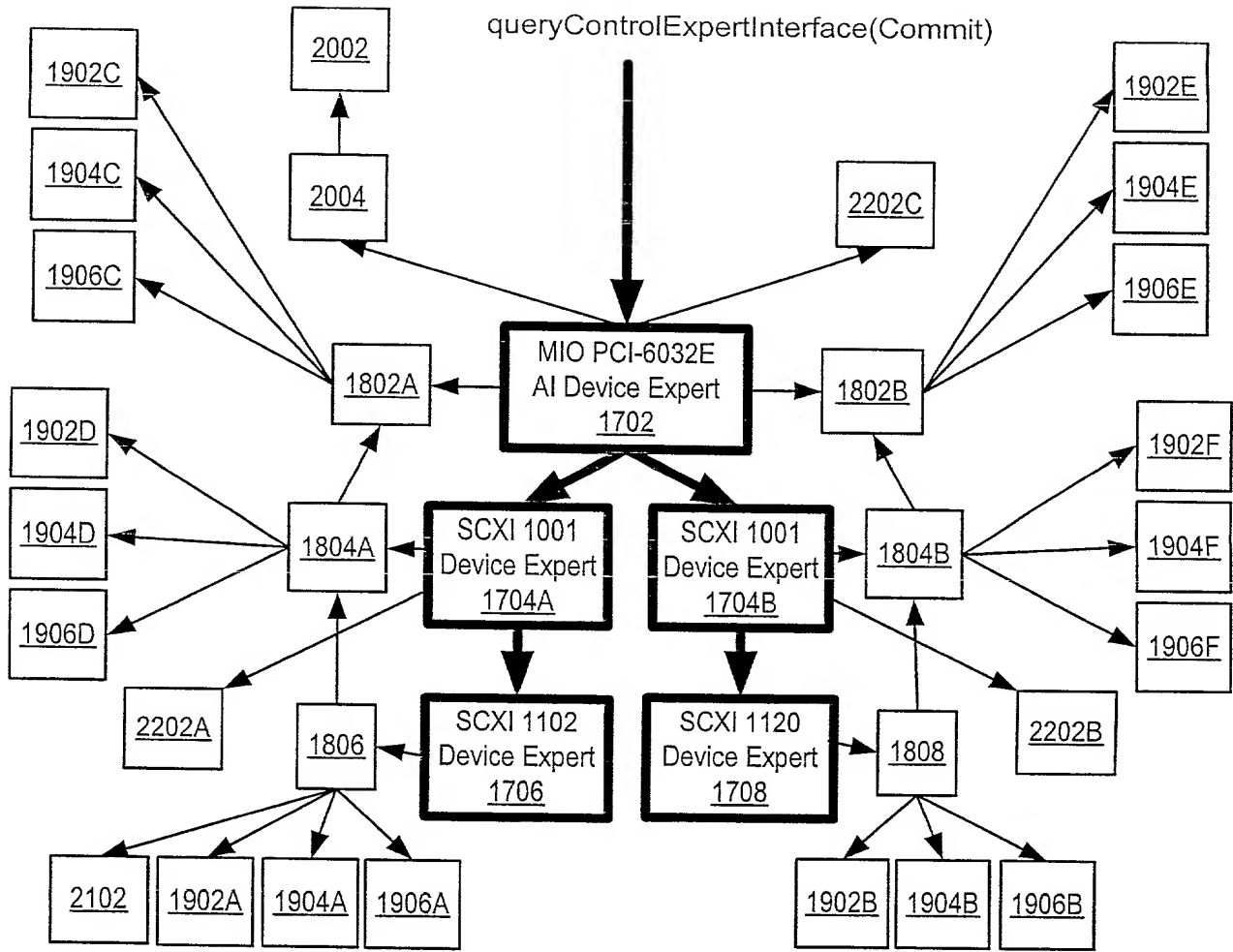


Figure 24A



Commit

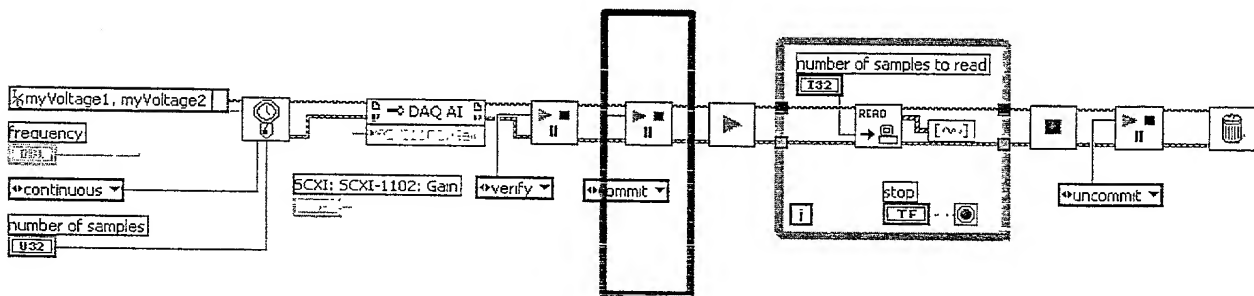
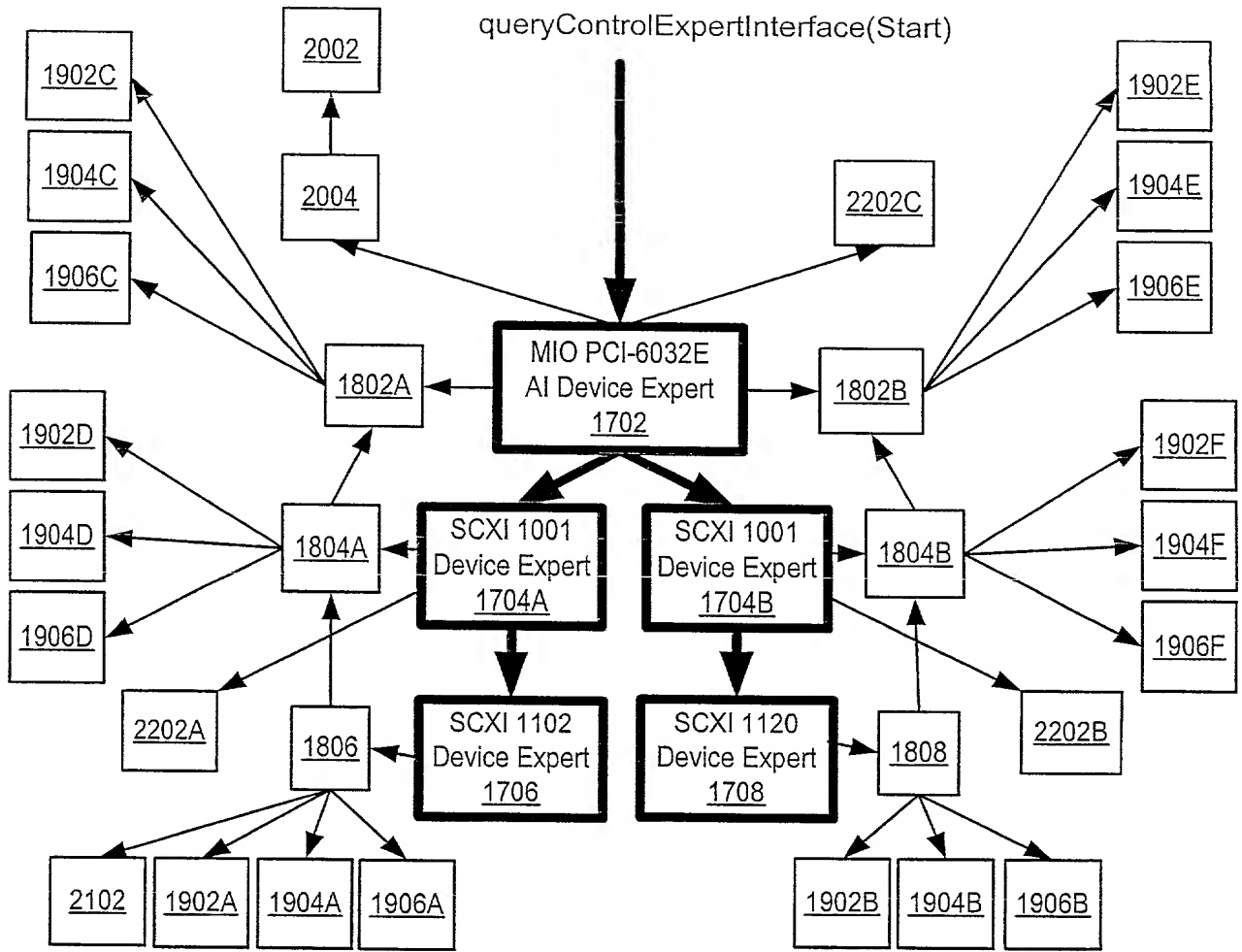


Figure 24B



Start

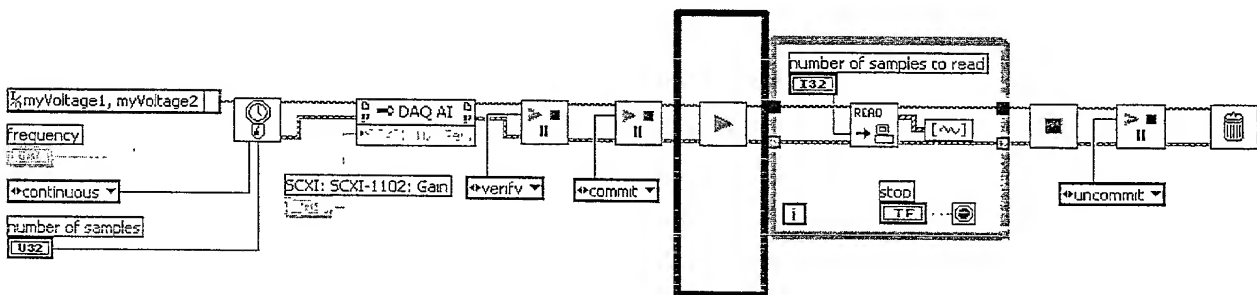
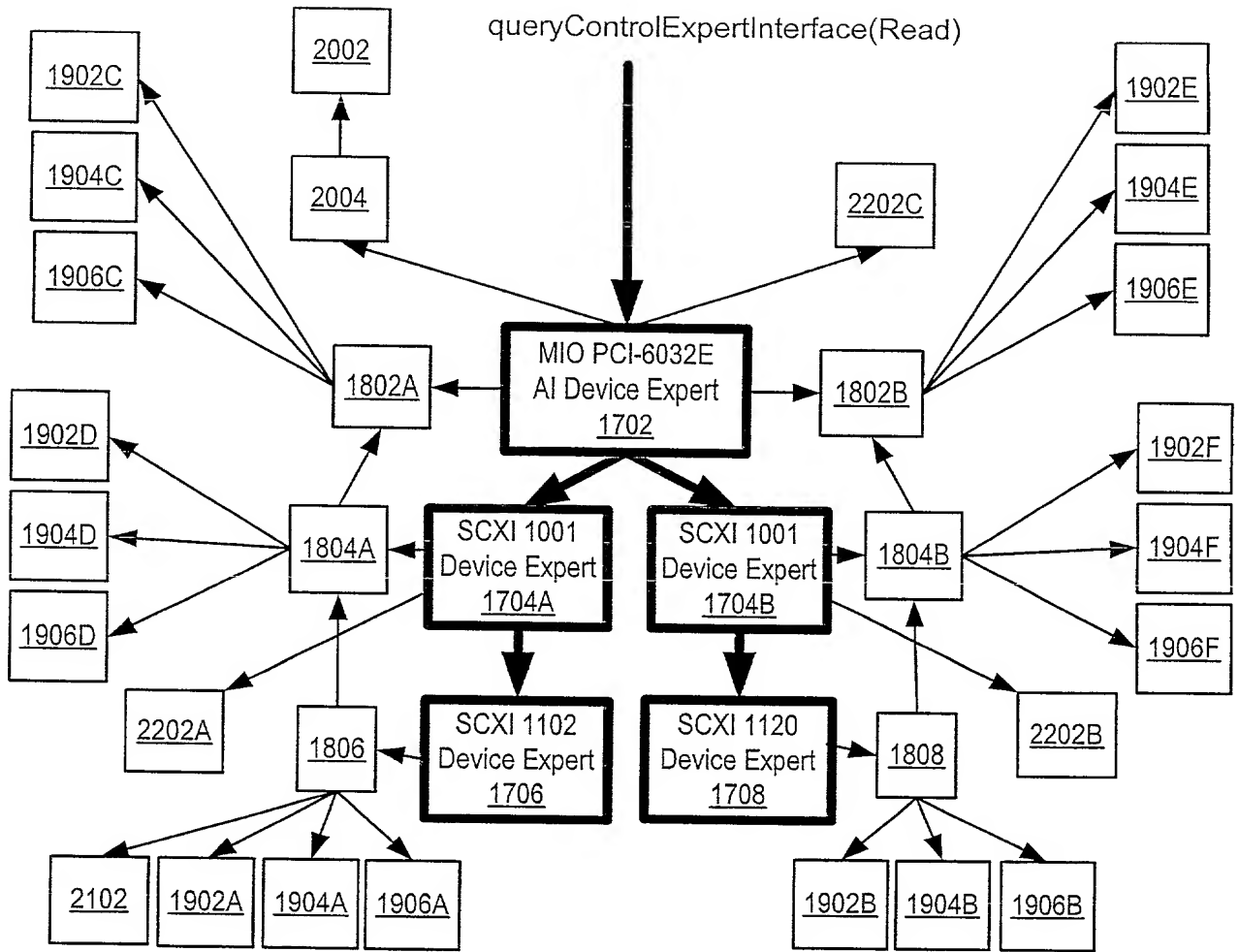


Figure 24C



Read

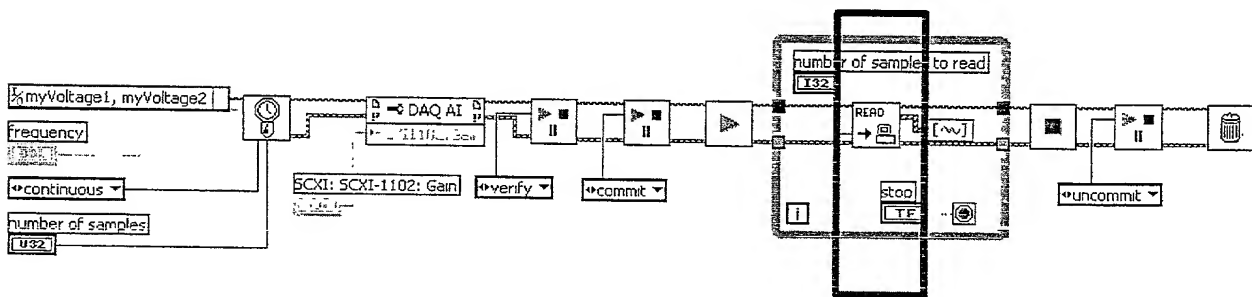


Figure 24D

Stop

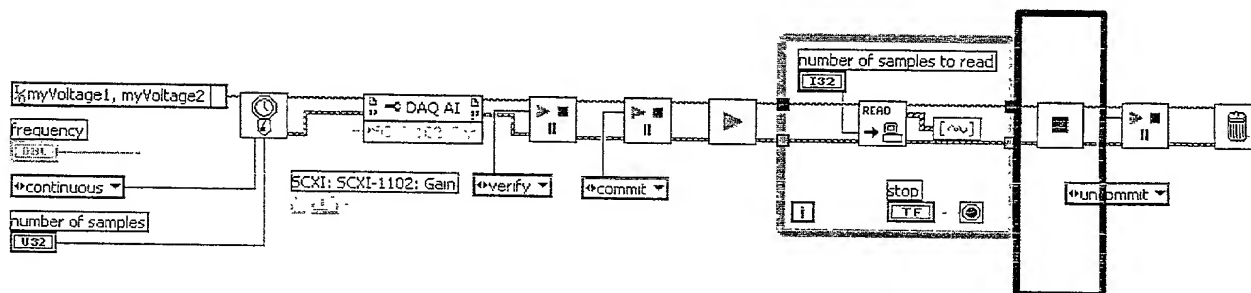
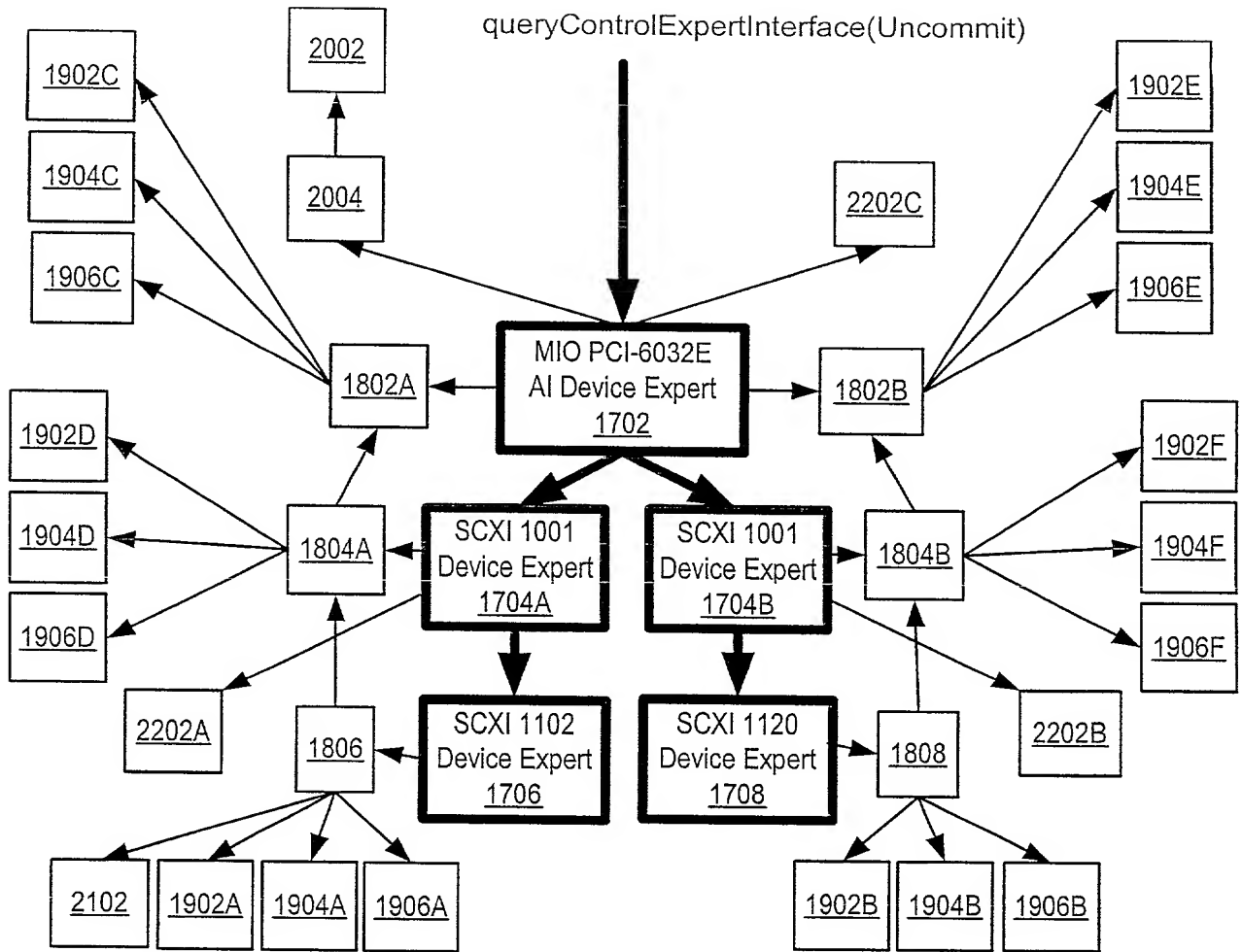


Figure 24E



Uncommit

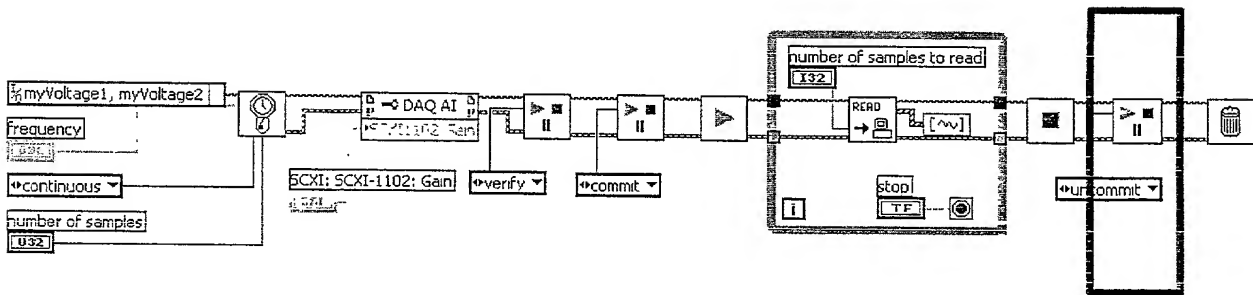


Figure 24F

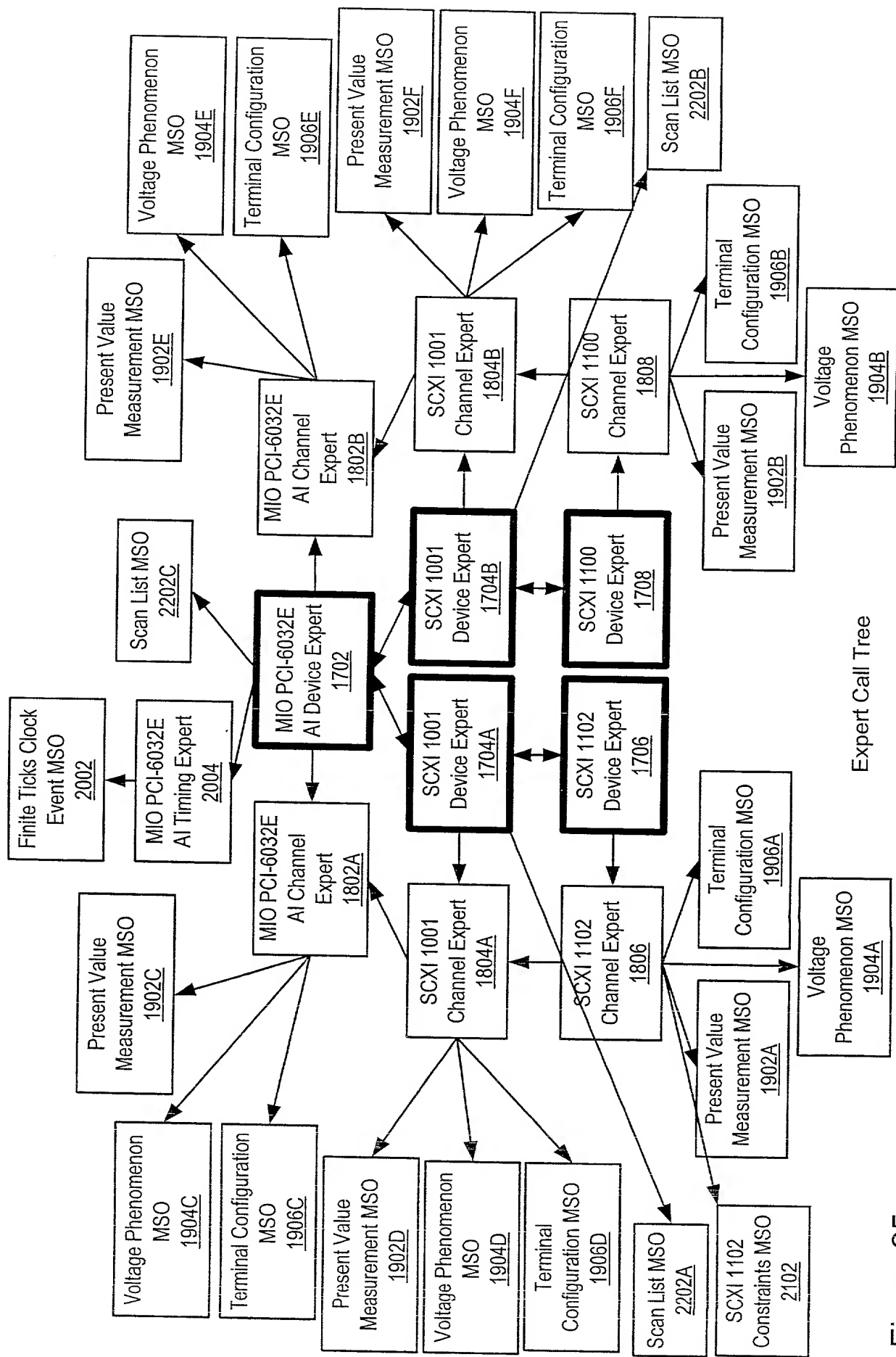


Figure 25

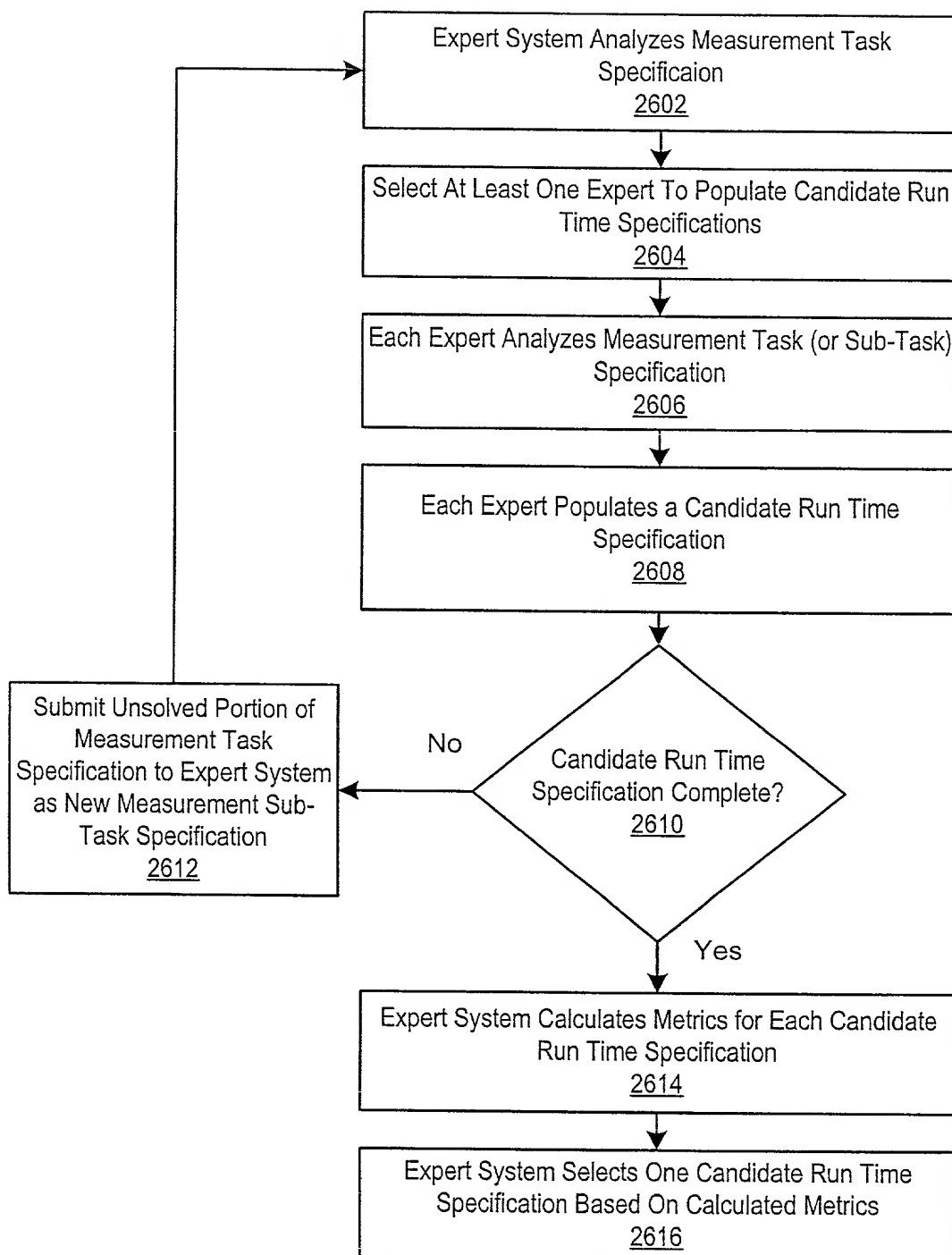


Figure 26

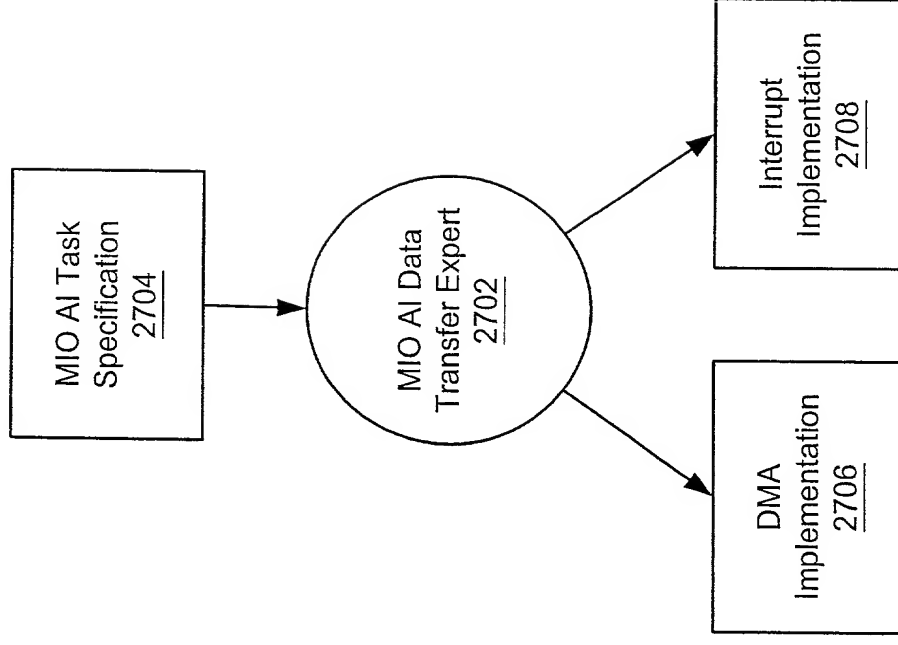


Figure 27

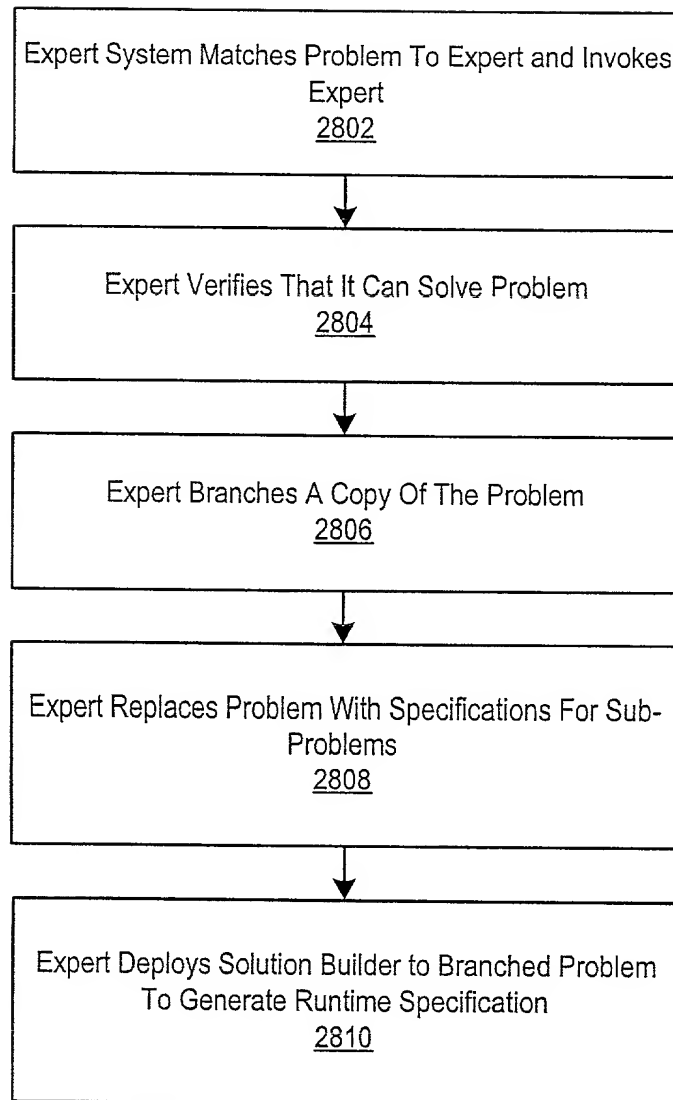


Figure 28

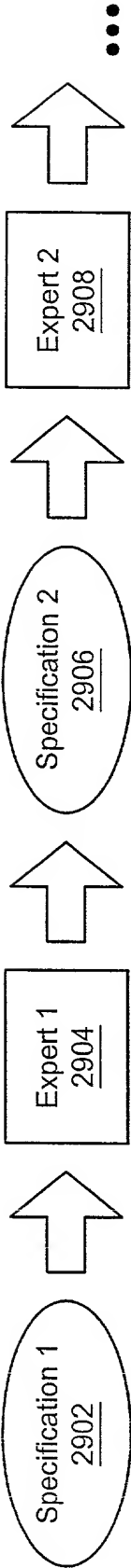


Figure 29

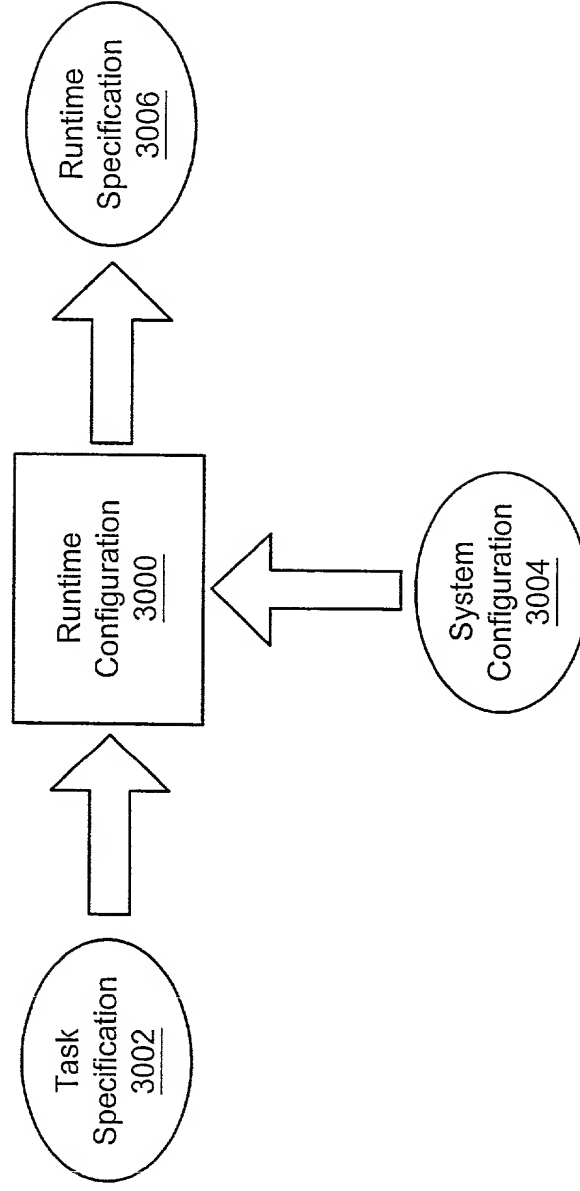


Figure 30

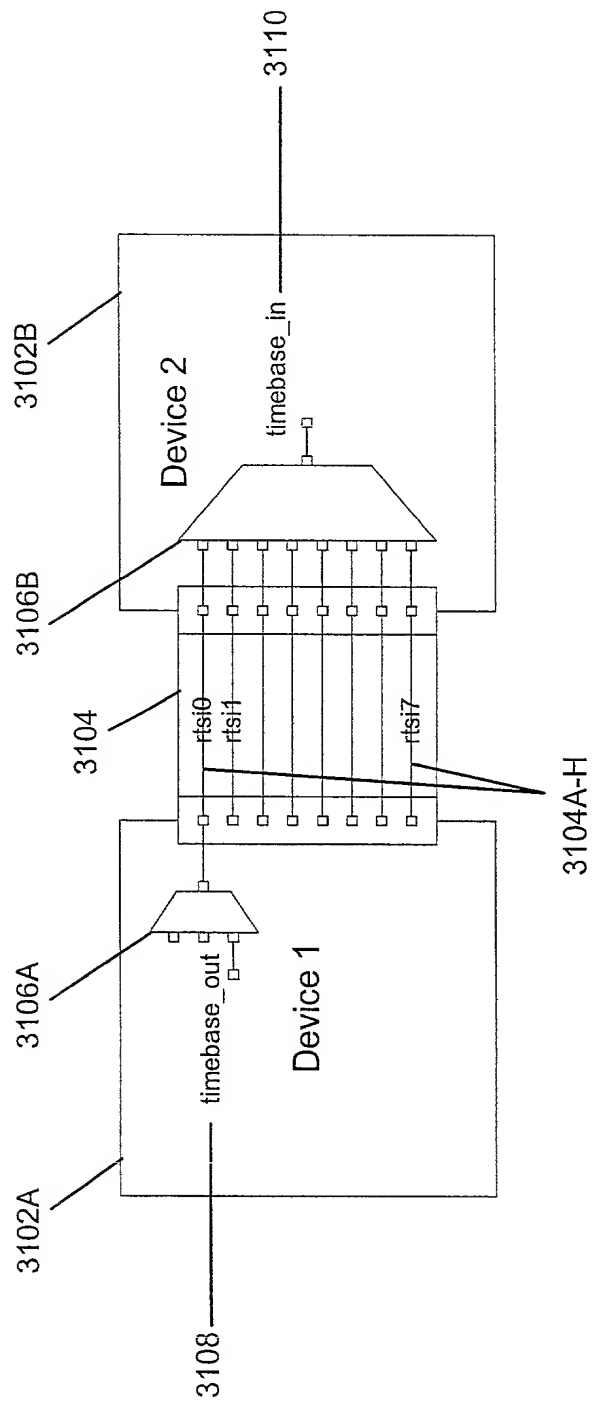


Figure 31

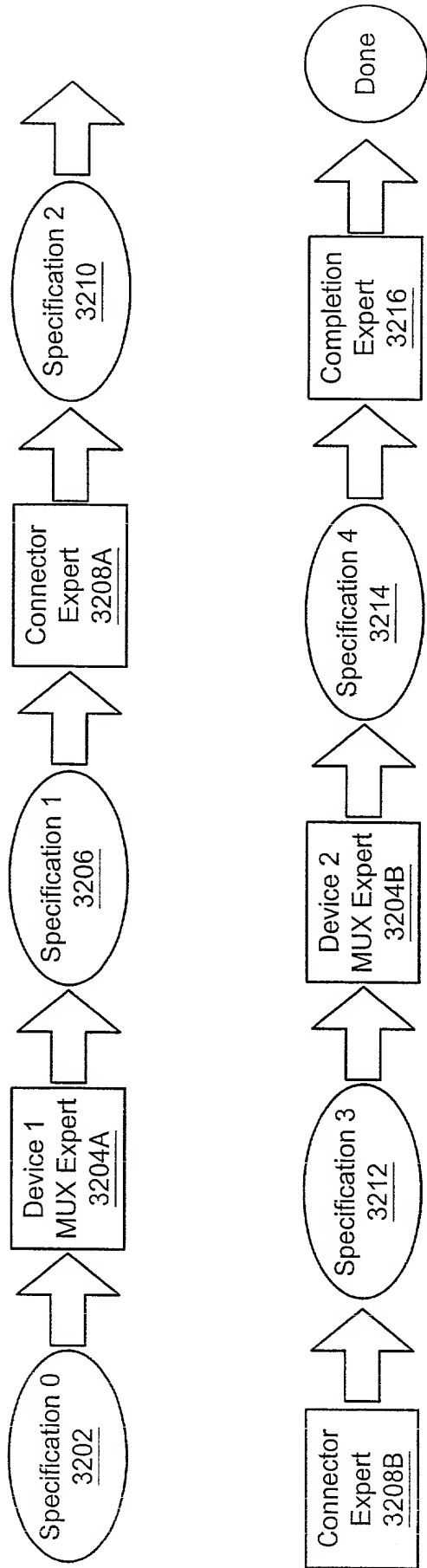


Figure 32

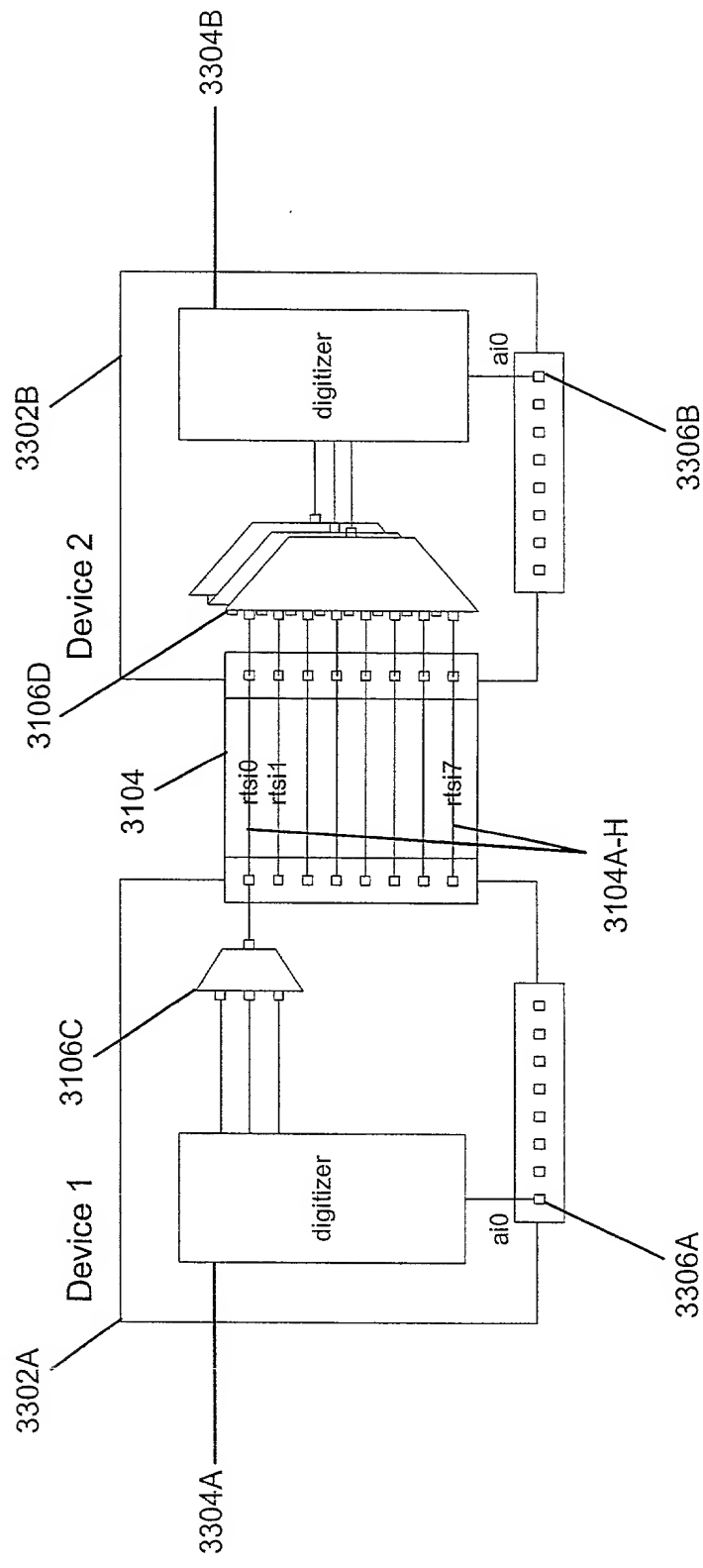


Figure 33

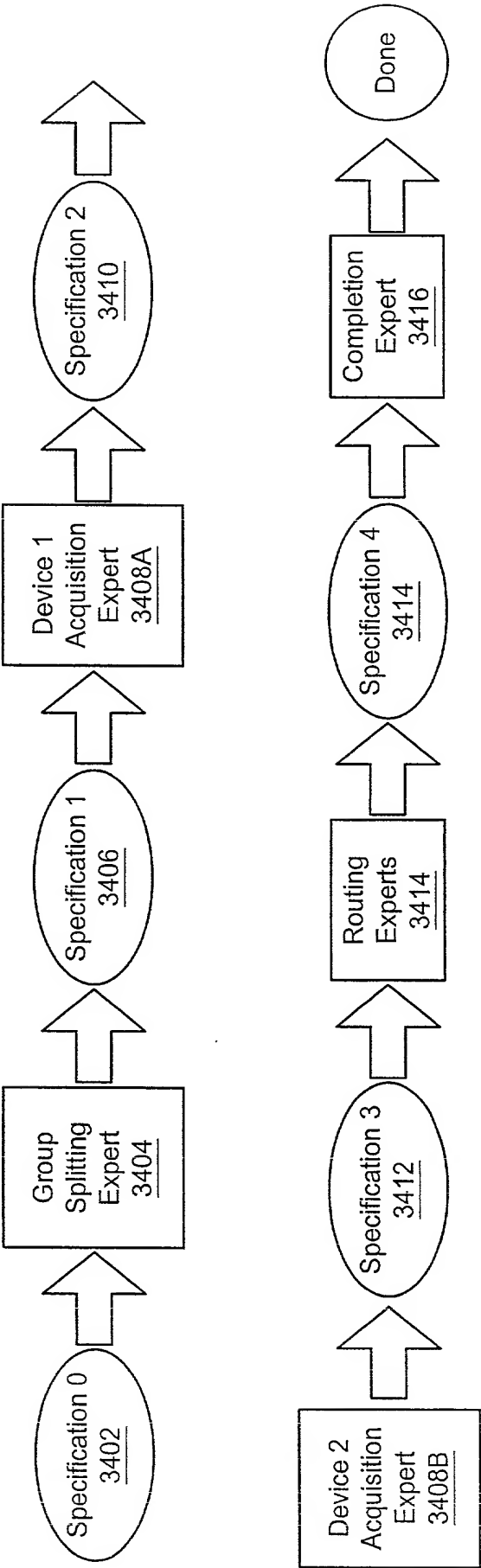


Figure 34

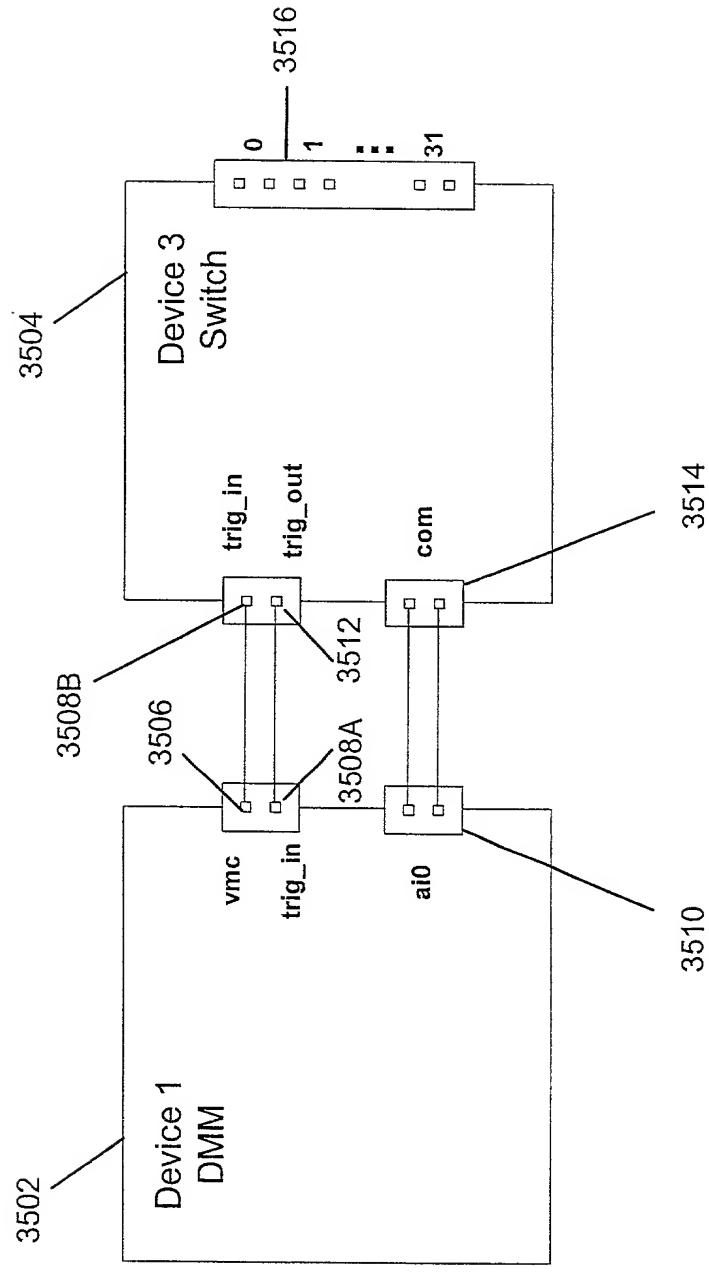


Figure 35

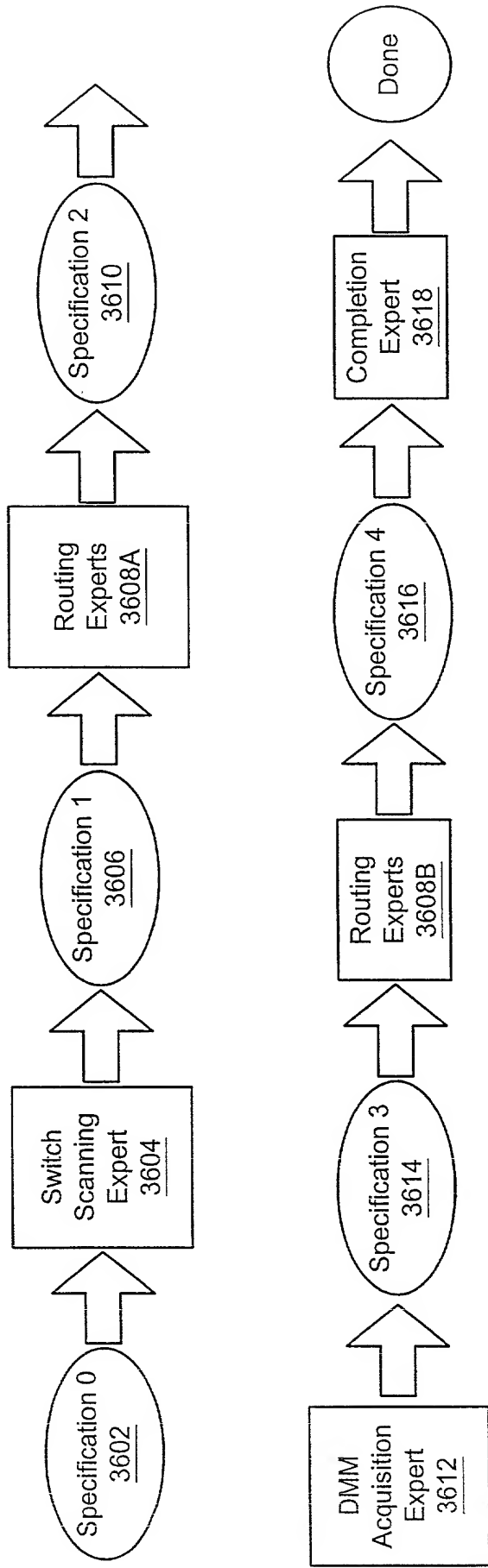


Figure 36

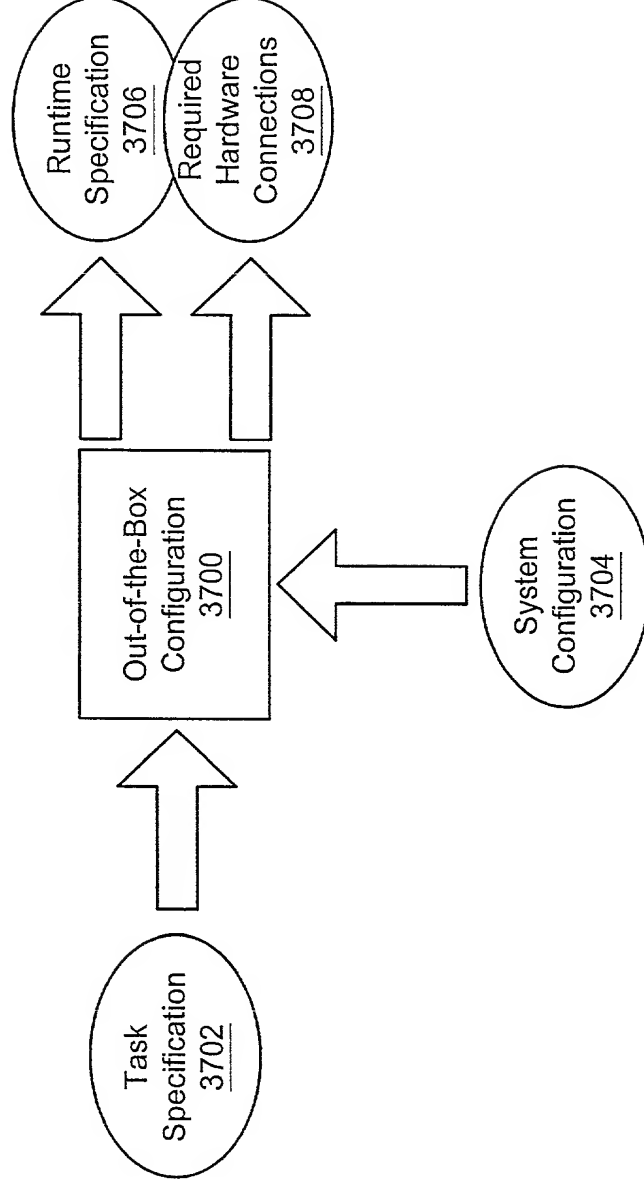


Figure 37

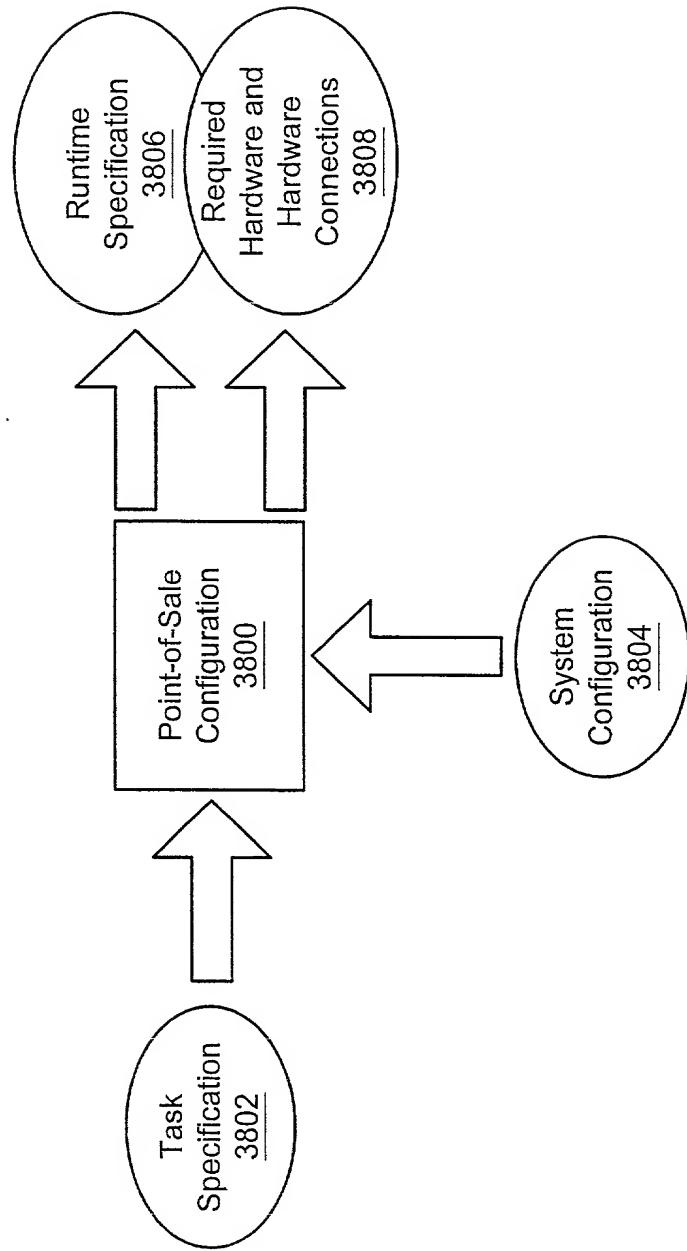
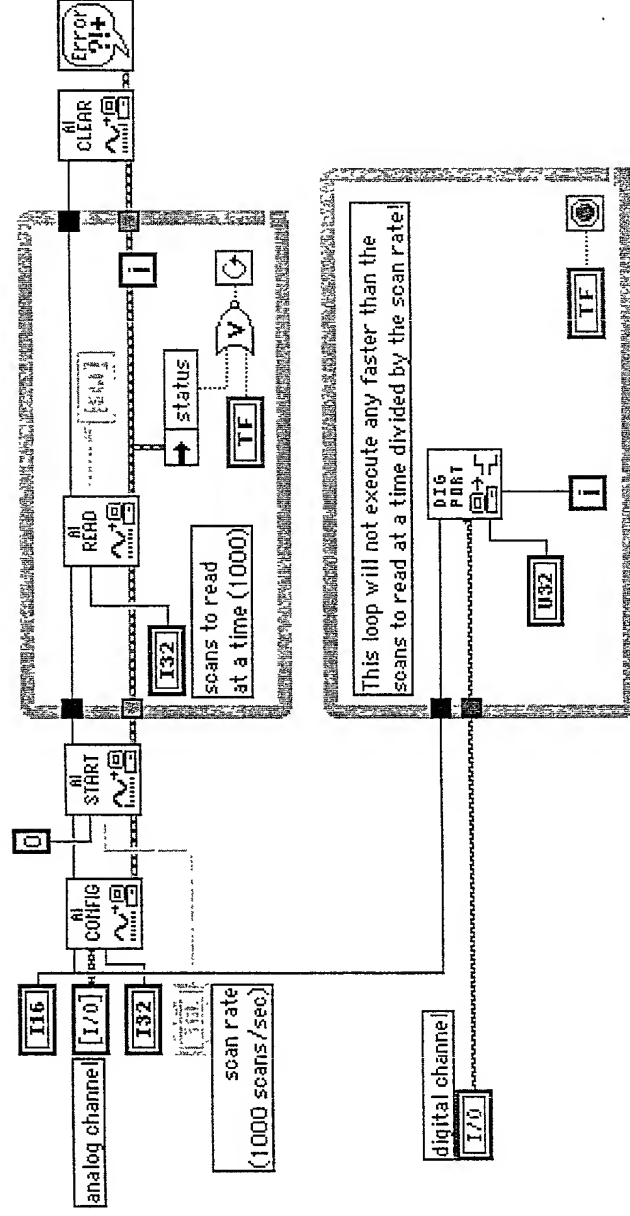
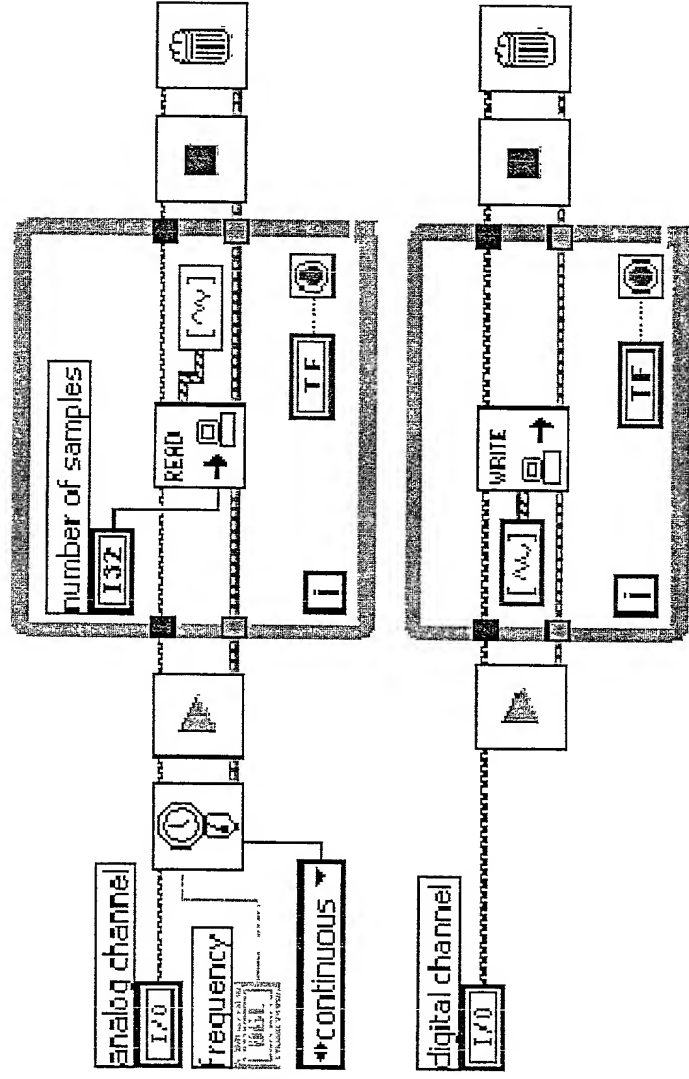


Figure 38



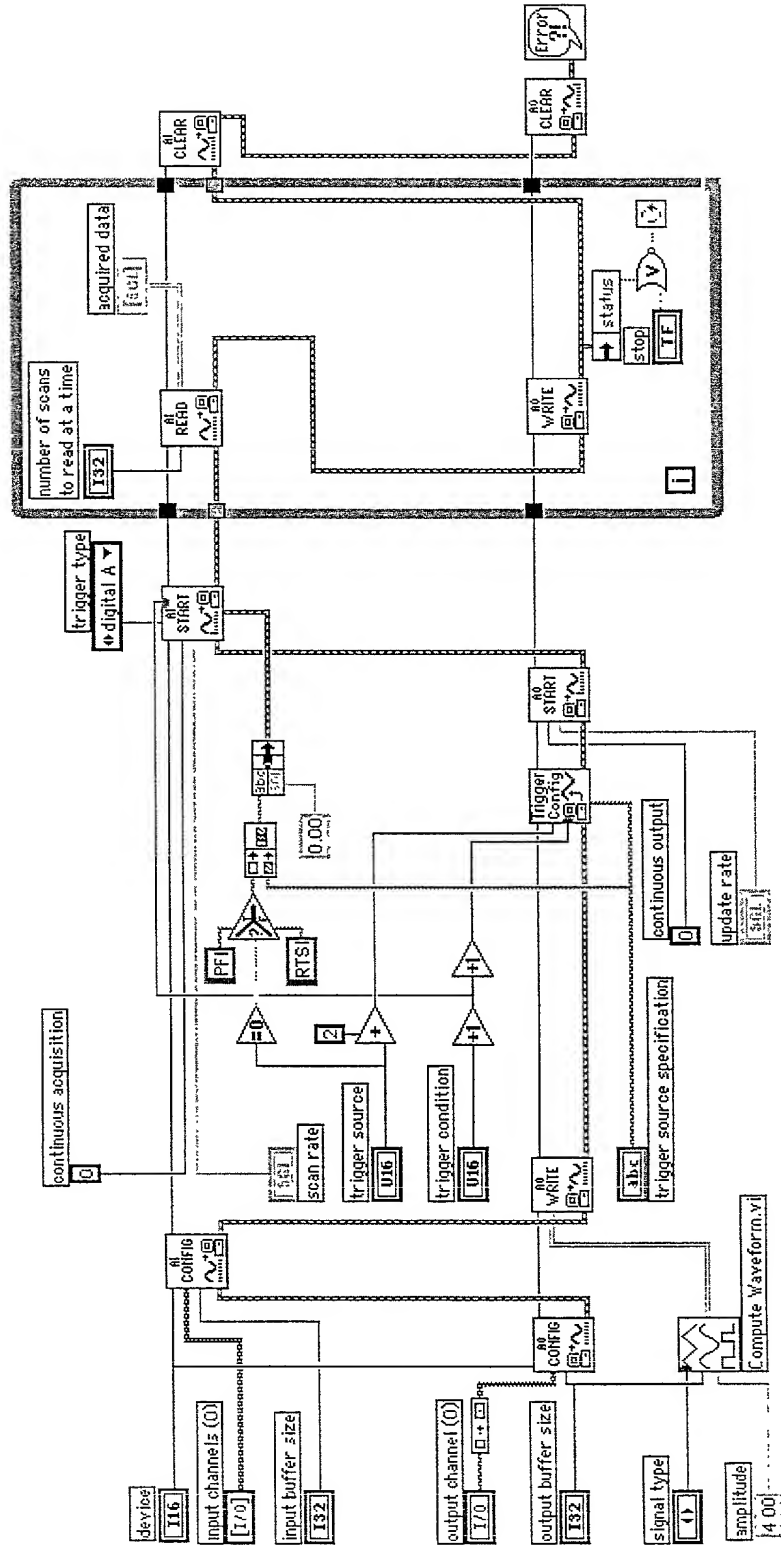
Simultaneous Buffered Analog Input And Single Point Digital Output With Single-Threaded Driver (Prior Art)

Figure 39A (Prior Art)



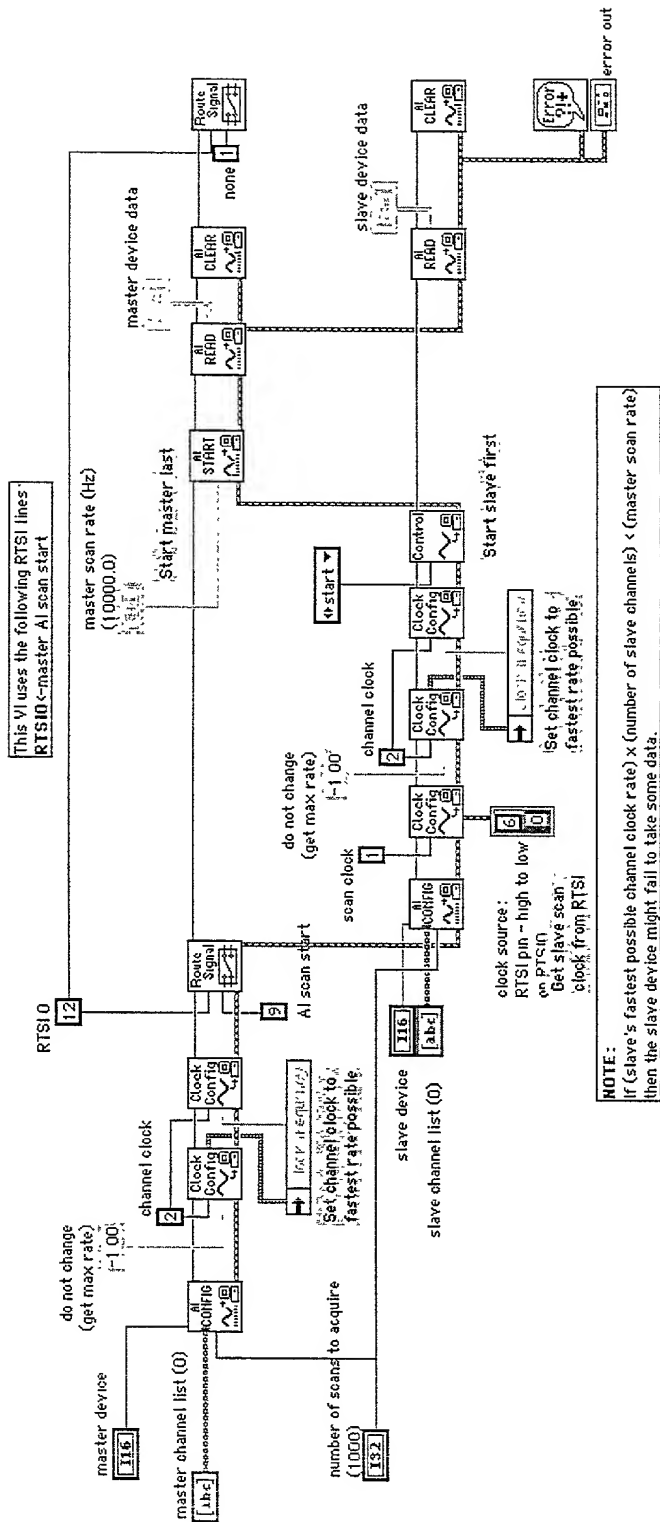
Simultaneous Buffered Analog Input And Single Point Digital Output With Multi-Threaded Driver

Figure 39B



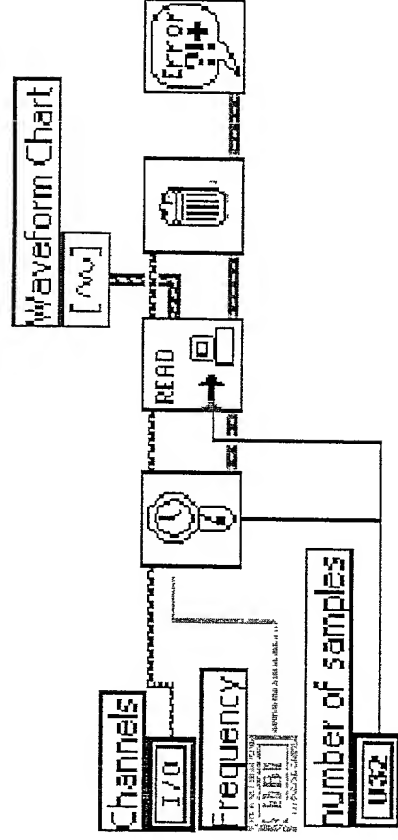
Simultaneous Triggered Buffered A/D AO (Prior Art)

Figure 40A



Sharing Scan Clock Across Two E-Series Devices (Prior Art)

Figure 41A



Sharing Scan Clock Across Two E-Series Devices

Figure 41B

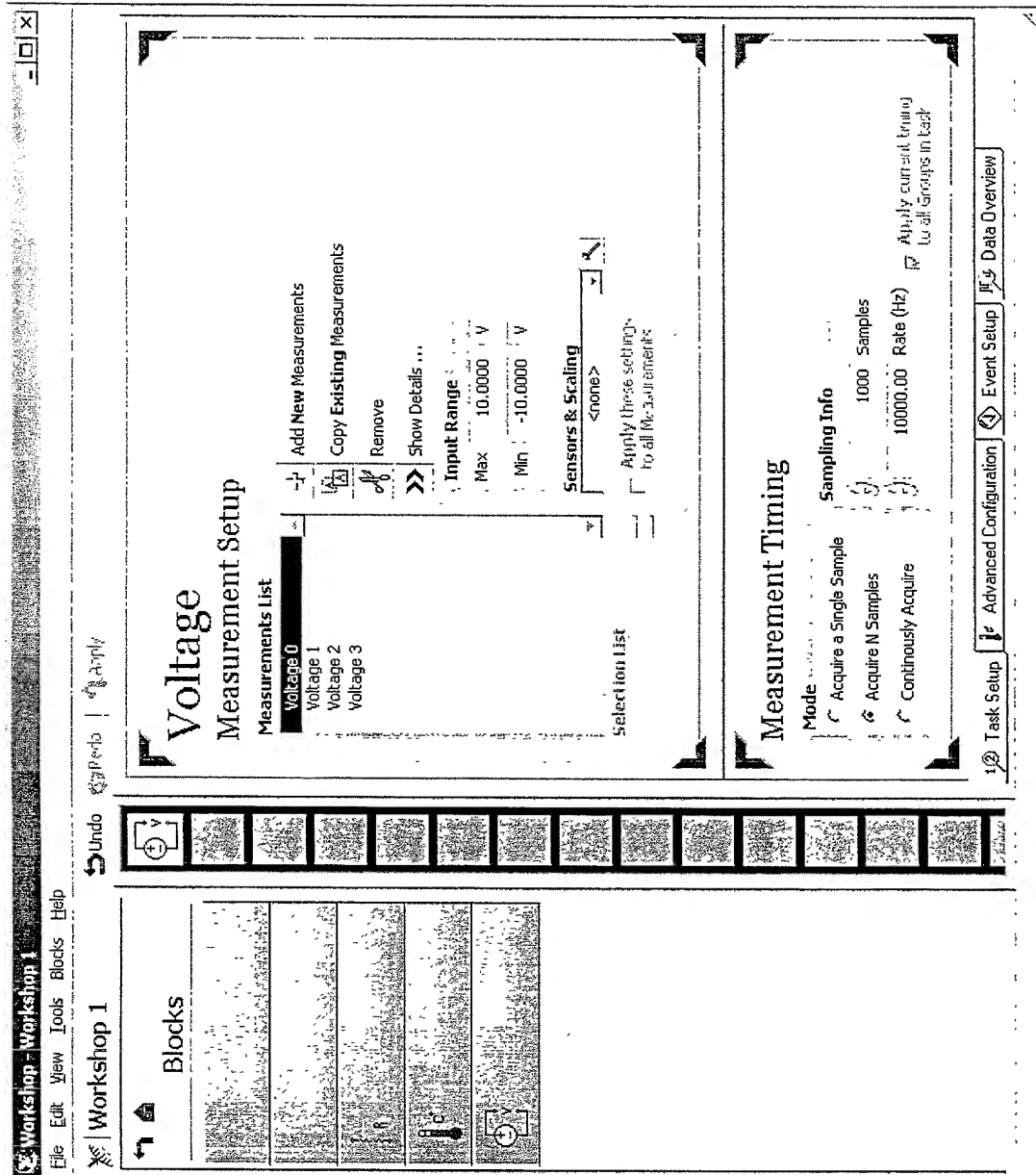


Figure 43B

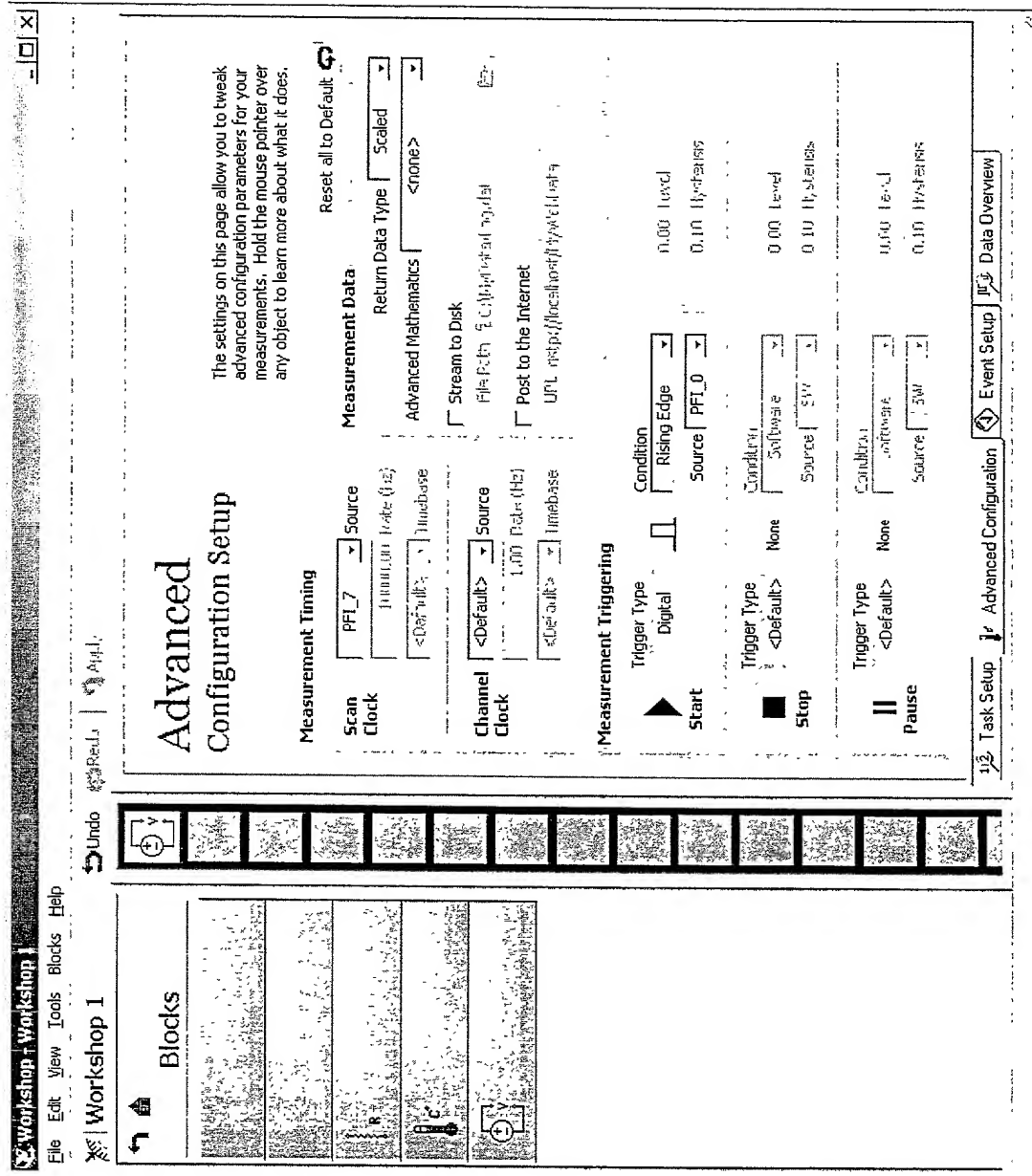
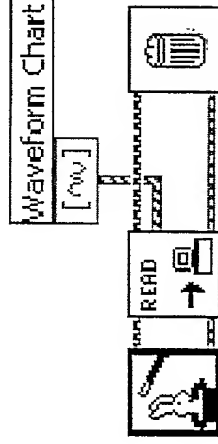
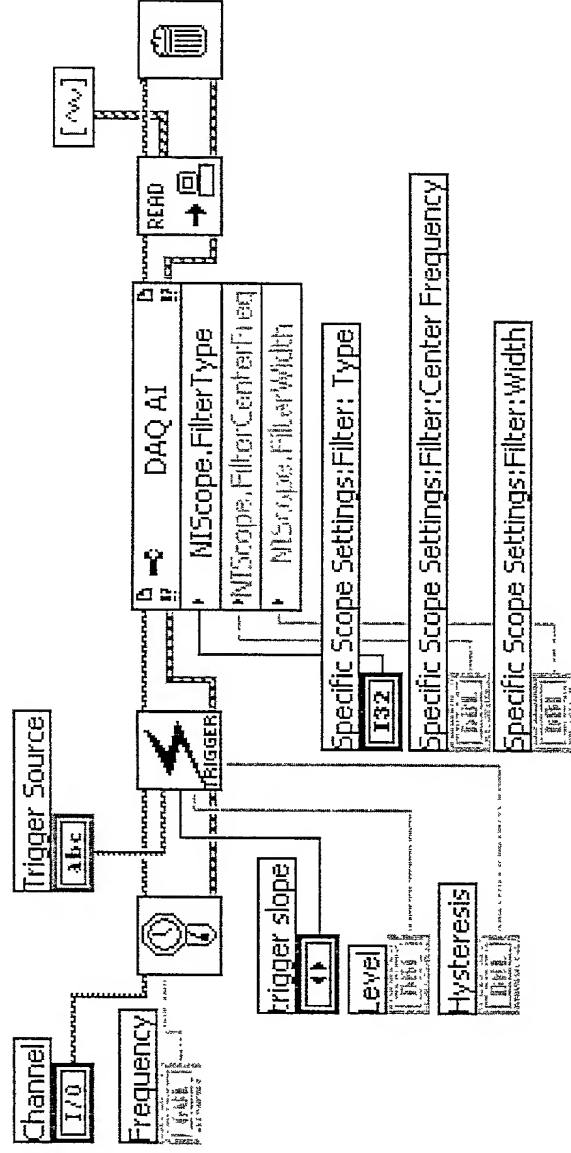


Figure 43C



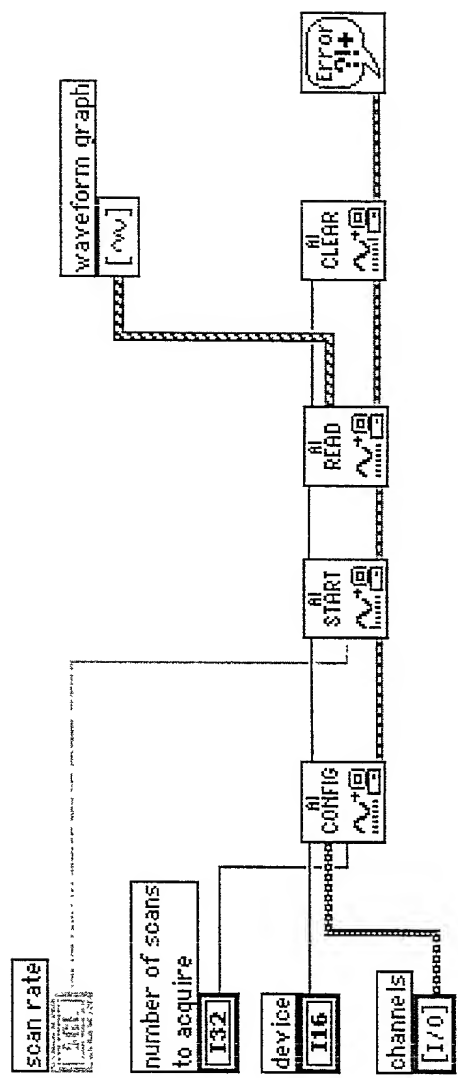
Acquire N Scans External Scan Clock Digital Trigger

Figure 43D



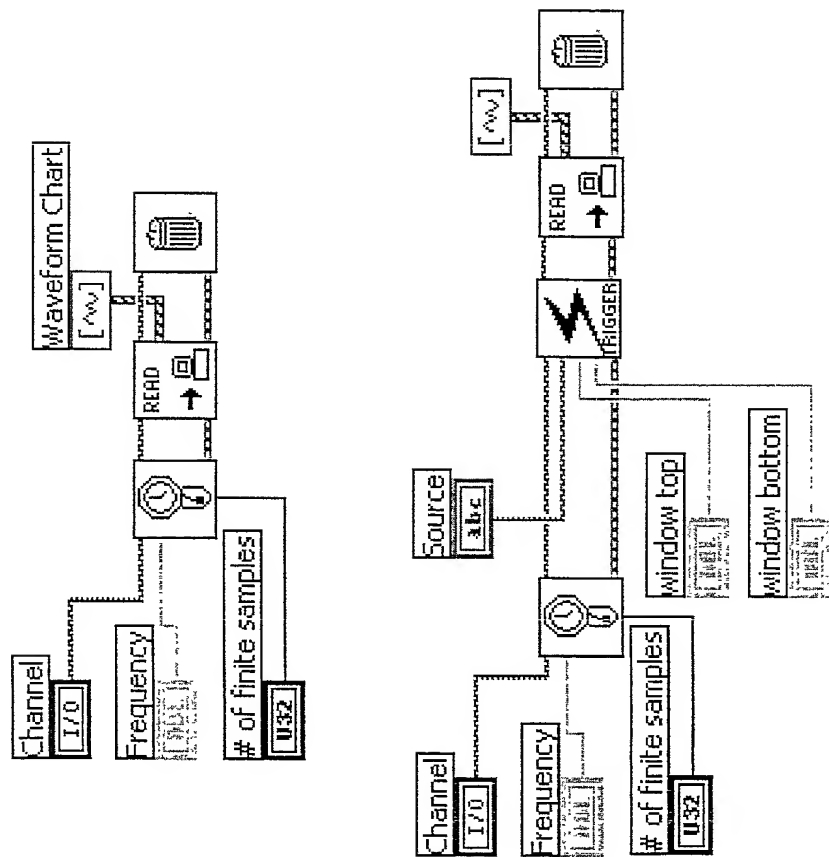
Triggered Acquisition With High Speed Digitizer With Filtering

Figure 44C



Intermediate Layer (Prior Art)

Figure 45A



Analog Window Triggering

Figure 45C